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INSTRUCTION MANUAL

MODEL 916XH

TWO CHANNEL SWEEP FREQUENCY RESPONSE ANALYZER

1 - INTRODUCTION

1.1 - PURPOSE

IT IS THE PURPOSE OF THIS INSTRUCTION MANUAL TO DESCRIBE THE MODEL 916 TWO CHANNEL SWEEP FREQUENCY RESPONSE ANALYZER.

MATERIAL IS PROVIDED WHICH DETAILS EVERY ASPECT OF THE MODEL 916'S OPERATION, APPLICATION, THEORY, CIRCUIT DESCRIPTION AND CALIBRATION PROCEDURE.

IF ANY OF THIS MATERIAL PROVES INADEQUATE TO YOUR NEEDS, PLEASE CONTACT US. WE ARE PREPARED TO ASSIST IN ANY ASPECT OF THE MODEL 916'S OPERATION AND APPLICATION BY YOUR ORGANIZATION.

1.1.1 - MODIFICATION OF THE 916 SPECIFICATION FOR 916XH

THE 916XH PERFORMANCE SPECIFICATION IS DEGRADED IN A SMALL WAY FROM THAT OF THE 916, IN THE 10 KHZ THRU 100 KHZ FREQUENCY RANGE.

THERE IS THE EQUIVALENT OF 50 MICROVOLT OF PICKUP AT 100 KHZ, DECREASING TO ZERO AT 10 KHZ IN EACH CHANNEL OF THE 916XH. THE 'WORSE CASE' EFFECT ON PERFORMANCE OF THE 916XH IN BOTH PHASE SHIFT AND AMPLITUDE IS SHOWN IN FIGURE 1-1.

ANYTIME THE 916XH IS BEING USED IN THIS ONE SMALL PORTION OF THE UPPER FREQUENCY RANGE, THE ERROR CAN BE COMPLETELY ELIMINATED BY PREAMPLIFICATION OF THE SIGNAL TO GREATER THAN 10 MV.

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1.2 - DISCLOSURE AND WARRANTY

BAFCO, INC. DOES NOT WARRANT THE RESULTS OBTAINED FROM ITS FREQUENCY RESPONSE ANALYZERS, AS BEING THE SOLE DETERMINANT IN A PRODUCTS' DESIGN, CHECKOUT, MAINTENANCE, OR CALIBRATION.

WHEREVER THE RESULTS OF A MEASUREMENT MADE WITH A BAFCO, INC. FREQUENCY RESPONSE ANALYZER, EFFECT PRODUCT SAFETY, PRODUCE DURABILITY OR PRODUCT SUITABILITY FOR HUMAN USE; THE RESPECTIVE ANALYZER'S RESULTS MUST BE CORROBORATED BY OTHER MEANS.

BAFCO, INC. DOES NOT ASSUME RESPONSIBILITY FOR THE CORRECTNESS OF CONCLUSIONS DRAWN FROM THE MODEL 916'S MEASUREMENTS, NOR FOR CONSEQUENTIAL DAMAGES.

SPECIFICATION CHANGES:

BAFCO, INC. RESERVES THE RIGHT TO DISCONTINUE ANY ITEM WITHOUT NOTICE, AND TO CHANGE SPECIFICATIONS OF ANY INSTRUMENT OR ANY PART AT ANY TIME WITHOUT INCURRING OBLIGATIONS TO INCORPORATE NEW FEATURES IN INSTRUMENTS OR PARTS PREVIOUSLY SOLD.

WARRANTY:

WE WARRANT EACH NEW INSTRUMENT MANUFACTURED BY US TO BE FREE FROM DEFECTS IN MATERIAL AND WORKMANSHIP. OUR OBLIGATION UNDER THIS WARRANTY SHALL BE LIMITED TO REPAIRING OR REPLACING AT OUR FACTORY ANY INSTRUMENT OR PART THEREOF WHICH WITHIN ONE YEAR AFTER SHIPMENT TO THE ORIGINAL PURCHASER, IS RETURNED TO US PREPAID AND WHICH OUR EXAMINATION SHALL DISCLOSE TO HAVE BEEN THUS DEFECTIVE. THIS WARRANTY IS EXPRESSLY IN LIEU OF ALL OTHER OBLIGATIONS OR LIABILITIES ON OUR PART, CONTRACTUAL OR OTHERWISE, EITHER TO THE ORIGINAL PURCHASER OR ANY OTHER PERSON. WE ASSUME NO LIABILITY FOR CONSEQUENTIAL DAMAGES OF ANY KIND EXCEPT WHERE THIS EXCLUSION IS PROHIBITED BY LAW AND THEN ONLY TO THE EXTENT THAT SUCH EXCLUSION IS PROHIBITED. THE PURCHASER, BY PLACING AN ORDER WITH US SHALL BE DEEMED TO ASSUME ALL LIABILITY FOR ANY AND ALL DAMAGES CONSEQUENTIAL UPON THE USE OR MISUSE OF THE EQUIPMENT BY THE PURCHASER, IT EMPLOYEES OR OTHERS. NO AGENT IS AUTHORIZED TO ASSUME FOR US ANY LIABILITY EXCEPT AS ABOVE SET FORTH. THIS WARRANTY APPLIES TO ALL BAFCO, INC. MANUFACTURED EQUIPMENT. THE WARRANTIES WE RECEIVE FROM THE ORIGINAL MANUFACTURER OF OTHER THAN BAFCO EQUIPMENT WILL BE PASSED ON TO THE PURCHASER.

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1.3 - WARNING - SAFETY PROCEDURES

THE FRONT PANEL OF THE 916 OPENS OUT FOR EASE OF CHECK-OUT AND ADJUSTMENT. LINE POWER (110 VOLT, A.C.) IS BROUGHT TO THE RIGHT FRONT PANEL BY WAY OF THE RIGHT HAND CABLE BOARD (BD. #19).

CARE SHOULD BE TAKEN IN HANDLING THE RIGHT FRONT PANEL.

IF BOARD #19 IS TO BE REMOVED FROM THE MODEL 916, DISCONNECT LINE POWER BEFORE HANDLING BOARD #19. LEAVE LINE POWER DISCONNECTED UNTIL ALL TEST SETUPS ARE COMPLETED.

IF BOARD #19 IS PUT ON AN EXTENDER, IT REQUIRES GREAT CARE TO KEEP HANDS OFF. TEST PROBES MUST BE USED EXCLUSIVELY. KEEP THE POWER LINE DISCONNECTED UNTIL THE BOARD #19 IS MOUNTED AND SECURE ON THE EXTENDER AND INTO THE ANALYZER.

IF ANY DOUBT EXISTS IN YOUR ORGANIZATION AS TO ITS COMPETENCE TO HANDLE BOARD #19 CHECKOUT, BAFCO, INC. WILL PERFORM THE WORK FOR YOU.

1.4 - ORGANIZATION

THE INSTRUCTION MANUAL IS ORGANIZED AS FOLLOWS:

SECTION 2 DESCRIBES THE FRONT PANEL CONTROLS, SWITCHES, POTS, AND METERS AND THE REAR PANEL BNC'S, SWITCHES AND CONNECTORS.

SECTION 3 PRESENTS OPERATING PROCEDURES FOR PUTTING THE MODEL 916 INTO OPERATION, FOR APPLYING IT TO FREQUENCY-BY-FREQUENCY MEASUREMENTS OF AMPLITUDE RATIO AND PHASE SHIFT, AND FOR USING THE MODEL 916'S SWEEP CAPABILITY TO SWEEP OVER THE FREQUENCY RANGE OF INTEREST WHILE PLOTTING AMPLITUDE RATIO (DB) AND PHASE SHIFT VS. LOG FREQUENCY.

SECTION 4 CONTAINS THE THEORY OF OPERATION OF THE MODEL 916. THIS INCLUDES A SEPARATE PRESENTATION OF EACH MAJOR SUBSYSTEM WITHIN THE FREQUENCY RESPONSE ANALYZER, AS WELL AS A PRESENTATION OF THE THEORY OF NOISE AND HARMONIC REJECTION.

SECTION 5 PRESENTS THE THEORY OF CIRCUIT OPERATION OF EACH PRINTED CIRCUIT BOARD.

SECTION 6 DESCRIBES THE MAINTENANCE AND CALIBRATION OF THE MODEL 916.

SECTION 7 GIVES A FAST CHECKOUT PROCEDURE FOR ASCERTAINING THAT THE MODEL 916 IS OPERATING SATISFACTORILY ALONG WITH A FAST CALIBRATE PROCEDURE FOR ADJUSTING THE MODEL 916 TO OPTIMUM OPERATING STATUS.

1.5 - AIDS TO USING THIS INSTRUCTION MANUAL

1.5.1 - DRAWINGS

DRAWING NO. B103400-1 IS A TABULATION OF ALL OF THE DRAWINGS ORGANIZED BY BOARD NUMBER.

DRAWING NO. C102927-1, SH. 2 & 3 SHOWS THE FRONT PANEL OF THE 916.

DRAWING NO. C102927-1, SH. 1 SHOWS THE FRONT OF THE 916 WITH THE FRONT DOOR OPEN.

DRAWING NO. C102927-1, SHS. 4 & 5 SHOWS THE REAR OF THE 916.

1.5.2 - OPERATIONAL AMPLIFIERS

IT IS ASSUMED THAT THE READER IS FAMILIAR WITH THE THEORY OF OPERATIONAL AMPLIFIERS. IF NOT, THE FOLLOWING REFERENCES ARE RECOMMENDED AS GIVING THE BASIC THEORY:

1) MODERN OPERATIONAL CIRCUIT DESIGN
BY J. I. SMITH - JOHN WILEY - 1971

2) NONLINEAR CIRCUITS HANDBOOK,
ANALOG DEVICES, 1974.

3) IC OP-AMP COOKBOOK
BY W. C. JUNG; H. W. SOMS & CO. - 1974

4) HANDBOOK OF OPERATIONAL AMPLIFIER APPLICATIONS
BURR-BROWN - 1963

5) OPERATIONAL AMPLIFIERS - DESIGN AND APPLICATIONS
MC GRAW-HILL - 1971.

1. - INTRODUCTION

1.5 - AIDS TO USING THIS INSTRUCTION MANUAL - CONT'D.

1.5.3 - DIGITAL LOGIC

C-MOS DIGITAL LOGIC BLOCKS HAVE BEEN USED THROUGHOUT.

WITH THE EXCEPTION OF BOARD #19, THE RIGHT HAND CABLE BOARD, AND THE CIRCUITS USED TO READ OUT THE DIGITAL METER OUTPUT, ALL OF THE C-MOS LOGIC IS BASED ON:

V_{DD} = GROUND = '+1' = ONE STATE

AND

V_{CC} = -15 VOLTS = '0' = ZERO STATE.

VOLUME 5, MCMOS INTEGRATED CIRCUITS, SERIES A, BY MOTOROLA SEMICONDUCTOR PRODUCTS, 1975, IS RECOMMENDED AS A SOURCE OF DETAILED DESCRIPTIVE MATERIAL ON EACH LOGIC ELEMENT.

1.5.4 - FETS

THROUGHOUT THE 916, THE FETS ARE USED AS SWITCHES. THEY ARE EITHER 'ON', OR 'OFF'. IN THE 'ON' STATE, THE GATE IS WITHIN 0.7 VOLTS OF THE DRAIN, AND THE SOURCE TO DRAIN RESISTANCE IS LOW (CONSIDER AS A SHORT). IN THE 'OFF' STATE, THE 'GATE' IS AT -15 VOLTS AND THE SOURCE TO DRAIN IS NEAR AN OPEN CIRCUIT.

THE DRAIN IS EITHER AT GROUND, OR AT THE MINUS INPUT OF AN OPERATIONAL AMPLIFIER WHICH IS KEPT NEAR GROUND POTENTIAL.

THE FET IS NEVER USED AS A VARIABLE RESISTOR, ONLY AS AN ON-OFF DEVICE.

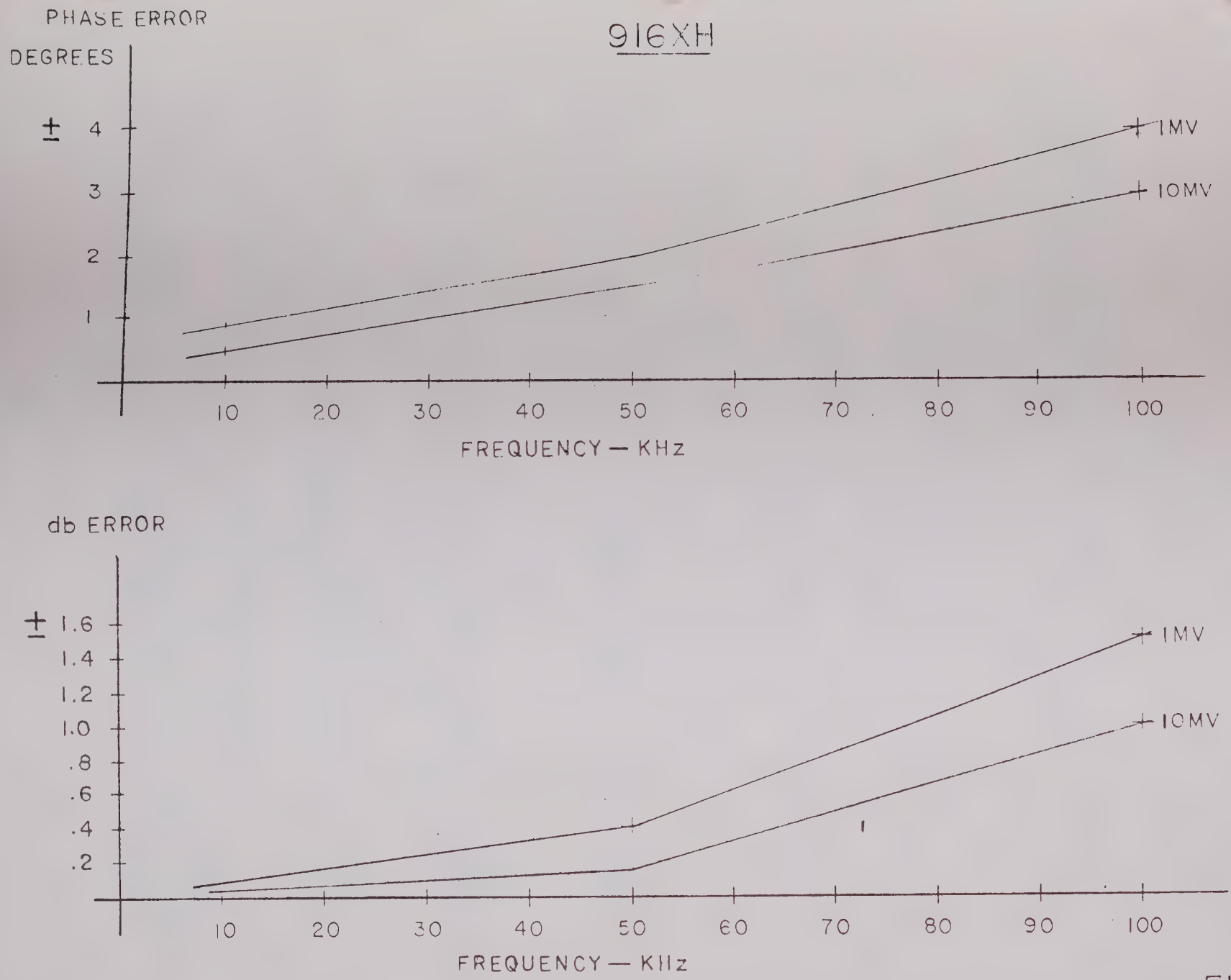
PHASE ERROR
DEGREES
916XH
± 4
3
2
1
1MV
10MV
10
20
30
40
50
60
70
80
90
100
FREQUENCY — KHz
db ERROR
± 1.6
1.4
1.2
1.0
.8
.6
.4
.2
1MV
10MV
10
20
30
40
50
60
70
80
90
100
FREQUENCY — KHz

FIG. 1-1

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916XH

2 - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS

REFERENCE: DRAWING NO. C102927-1, SH. 3

2.1.1 - RETURN SIGNAL CONNECTIONS & CONTROLS

J1A, J2A - BNC'S FOR RETURN SIGNAL '+' & '-' CHANNEL #2. FOR SINGLE ENDED INPUTS, GROUND UNUSED BNC.

J3A, J4A - BNC'S FOR RETURN SIGNAL '+' & '-' CHANNEL #1. FOR SINGLE ENDED INPUTS, GROUND UNUSED BNC.

S12 - FAST D.C. REJECT CH. #2.

S11 - FAST D.C. REJECT CH. #1.

MOMENTARY SWITCHES TO GROUND INPUT CONDENSERS (TO SPEED-UP THEIR CHARGING TO RETURN SIGNAL DC OFFSET). USE AT INITIAL CONNECTION TO A LARGE DC OFFSET; OR IMMEDIATELY AFTER A LARGE CHANGE IN OPERATING POINT.

S10 - PRESET GAIN

MOMENTARY SWITCH SETS HIGH GAIN IN AUTOMATIC GAIN CONTROL OF INPUT AMPLIFIER. WHEN RELEASED, SPEEDS UP AUTOMATIC GAIN CONTROL'S ACTION TO OPTIMUM GAIN. USE AT FIRST CONNECTION, ONLY.

S13 - FILTER - 'IN-OUT'

ADDS MATCHED LOW PASS FILTER ACTION TO BOTH CHANNELS. BREAK FREQUENCY (SINGLE POLE) AT 10,000 HZ. REDUCES EFFECT OF VERY HIGH FREQUENCY NOISE.

S15 - 'X5' INTEGRATE - 'IN-OUT'

INCREASES INTEGRATE TIME BY 5/1 IN FREQUENCY RANGES 3, 4, 5 & 6 (FROM 10 HZ THRU 100,000 HZ) AND BY 2/1 IN FREQUENCY RANGES 1 & 2 (FROM .05 HZ THRU .10 HZ). USE TO INCREASE NOISE REJECTION. REQUIRES SLOWER SWEEP SPEED FOR SAME NUMBER OF POINTS ON PLOT.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.2 - ANALYZER CONDITION INDICATIONS

DS6 & 7 - CH. #2 UNDERLOAD & OVERLOAD

DS4 & 5 - CH. #1 UNDERLOAD & OVERLOAD -

ENERGIZED WHEN THE RESULT OF THE LAST ANALYSIS CYCLE WAS A SIGNAL UNDERLOAD OR OVERLOAD. GAIN IS AUTOMATICALLY CHANGED 2/1 TO REMOVE OVERLOAD OR UNDERLOAD IN THE NEXT CYCLE OF ANALYSIS.

OVERLOAD ALSO ENERGIZED BRIEFLY FOR NOISE SPIKES. ANALYSIS CYCLE IS ABORTED AND RESTARTED AT 1/2 THE GAIN.

PRESENCE OF ENERGIZED UNDERLOAD LIGHT AND FLASHING OVERLIGHT LIGHT INDICATES THAT THE S/N RATIO EQUALS 1/8 (OR WORSE).

SEE SECTION 3 FOR RECOMMENDATIONS.

CONTINUED UNDERLOAD LIGHT INDICATES INPUT SIGNAL COMPONENT UNDER 4.0 MV. AUTOMATIC GAIN CONTROL CANNOT REMOVE, AS THE MAXIMUM GAIN IS ALREADY PRESENT.

2.1.3 - FREQUENCY OF POINT-BY-POINT OPERATION

(OR START FREQUENCY OF SWEEP) -

R1, S1 - SET FREQUENCY RANGE (FULL SCALE) BY DEPRESSING ONE OF S1A TO S1E INTERLOCKED SWITCHES.

SET FREQUENCY ON 'R1' AS A FRACTION OF FULL SCALE (.050 TO 1.000) DIRECT READING. FOR PRECISION, USE M2 FOR FREQUENCY READING (WITH S17B DEPRESSED).

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.4 - SWEEP OPERATION

R2, S2 - STOP FREQUENCY -

S2A THRU S2F FOR FREQUENCY RANGE (FULL SCALE), AND 'R2' AS A FRACTION OF FULL SCALE (FROM .100 THRU 1.000).

S3, S4 - SWEEP SPEED -

FULL SCALE SEC/DECADE OF 10^4 (100,000), 10^3 (10,000), 10^2 (1,000), 10^1 (10) SEC. PER DECADE FOR S3 SETTING OF N = 4, 3, 2, 1, RESPECTIVELY.

FRACTION OF FULL SCALE SET BY S4 AT X1.0, X.8, X.6, X.4, X.2. THUS, TO SET 800 SEC/DECADE, USE N = 3, X.8 (1000X.8).

SWEEP SPEED (ON EITHER OR BOTH SWITCHES) MAY BE ALTERED AS THE SWEEP OCCURS.

S9, S14 - SWEEP MODE -

S9 IN RESET, (S9A DEPRESSED) CAUSES OPERATION AT THE 'START' FREQUENCY (SETTING OF R1, S1).

S9 IN 'SWP', (S9B DEPRESSED) MAKES ANALYSIS FREQUENCY INCREASE CONTINUOUSLY FROM THE 'START' TO THE 'STOP' FREQUENCY SETTINGS ON A LOG SWEEP BASIS AT THE SET SWEEP SPEED.

S9 IN 'HOLD' (S9C DEPRESSED) STOPS THE SWEEP AT ITS OPERATING FREQUENCY AND HOLDS IT THERE (USE FOR SHORT-TIME HOLD). RETURNING TO 'S9B' DEPRESSED (SWP) CONTINUES THE SWEEP WITHOUT A TRANSIENT.

S14 IS A MOMENTARY SWITCH. WHEN DEPRESSED AND WITH S9B DEPRESSED, THE SWEEP SENSE IS REVERSED (SWEEPS DOWN IN FREQUENCY) AT ABOUT 1/2 THE SWEEP UP RATE. USE TO RETRACE A SMALL PORTION OF PLOT. S14 CANNOT BE USED TO SWEEP DOWN TO A LOWER FREQUENCY RANGE.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.4 - SWEEP OPERATION - CONT'D.

DS8, DS2, DS9, DS3 - SWEEP STATUS -

DS8 IS ENERGIZED WHEN SWEEP MODE IS RESET (S9A DEPRESSED). IT INDICATES TESTING ONE FREQUENCY AT A TIME, OR AT 'START' OF SWEEP.

DS2

IS ENERGIZED DURING SWEEP.

DS9

IS ENERGIZED WHEN SWEEP HAS REACHED 'STOP' FREQUENCY.

DS3

IS ENERGIZED WHEN SWEEP GOES INTO 'HOLD'. THIS IS DUE TO S9C BEING DEPRESSED, OR S5 PUT INTO 'OFF', OR DUE TO NOISE OVERLOAD (SHORT FLASH), OR DUE TO FREQUENCY RANGE SWITCH (SHORT FLASH).

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2 - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.5 - TEST SIGNAL AMPLITUDE, OFFSET, WAVESHAPE, & ON-OFF

S6 - WAVESHAPE -

S6 SELECTS WAVESHAPE OF THE TEST SIGNAL AS SQUARE (S6A), TRIANGLE WAVE (S6B), SINE WAVE (S6C).

S7 - R3 - AMPLITUDE -

FULL SCALE IS SET AT 10.0 VOLT PEAK (20 VOLTS PEAK-TO-PEAK) BY S7A AND 1.0 VOLT PEAK BY S7B.

R3 IS A MUTLIPLIER OF .000 TO 1.000 ON THE SETTING OF S7.

THUS, A .650 VOLT PEAK TEST SIGNAL IS SET BY DEPRESSING S7B, AND SETTING R3 AT .650.

J5A - BNC

OUTPUT TEST SIGNAL. ALSO AVAILABLE ON J5B OF REAR PANEL.

R4, S8 - D.C. OFFSET -

SELECT ZERO OFFSET (DEPRESS S8C), OR POSITIVE OFFSET (DEPRESS S8B), OR NEGATIVE OFFSET (DEPRESS S8A).

SET OFFSET LEVEL IN SELECTED POLARITY USING R4. READ PRECISELY ON M1 WITH DEPRESSED, AND S5 'OFF'.

OFFSET SWITCH S8 MAY ALSO BE USED FOR PRECISE STEP INPUT.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.5 - TEST SIGNAL AMPLITUDE, OFFSET, WAVESHAPE, & ON-OFF - CONT'D.

S5 - ON-OFF -

DEPRESS 'ON'. ANALYZER IN FULL OPERATION. SINE WAVE TEST SIGNAL STARTS FROM ZERO, TRANSIENT FREE.

RELEASE 'OFF'. TEST SIGNAL IS RESET TO ZERO. ANALYZER IS RESET, BUT THE RESULTS OF THE LAST COMPLETE ANALYSIS CYCLE IS LEFT ON THE OUTPUTS. IF IN SWEEP, SWEEP GOES INTO 'HOLD'.

USE FOR EMERGENCY TURNING OFF OF TEST SIGNAL, AND FOR 'QUICK-LOOK' ANALYSIS (RESULTS IN 2 OR 3 CYCLES OF ANALYSIS WITH S5 'ON').

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.6 - METER READOUTS - & SELECTOR SWITCHES

M1, S16 -

M1 IS A 3 1/2 DIGIT, BIPOLAR READOUT. S16 SELECTS THE READING AS:

S16A - AMPLITUDE CH. #2 IN DB

0.0 DB = 1 VOLT PEAK (OF FUNDAMENTAL)

-20.0 DB = .1 VOLT PEAK; ETC.

S16B - AMPLITUDE CH. #1 IN DB

SAME AS S16A.

S16C - AMPLITUDE RATIO -

CH#2/CH#1 IN DB (RATIO OF FUNDAMENTAL COMPONENTS)

0.0 DB = GAIN OF 1/1 = 1

+20.0 DB = 10/1;

-20.0 DB = 1/10; ETC.

S16D - OFFSET

M1 READS THE D.C. OFFSET IN THE OUTPUT TEST SIGNAL. AT LOWER FREQUENCIES, PUT S5 'OFF' TO OBTAIN A READING.

M2, S17, DS11, DS12 & DS13

M2 IS A 3 1/2 DIGIT BIPOLAR READOUT. S16 SELECTS THE READING AS:

S17A - PHASE SHIFT - (CH#2 - CH#1) IN DEGREES, TO ±180.0 DEGREES

2 - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.1 - FRONT PANEL CONTROLS, BNC'S & READOUTS - CONT'D.

2.1.6 - METER READOUTS & SELECTOR SWITCHES - CONT'D.

S17B - FREQUENCY: DS11, DS12, DS13

FREQUENCY READS OUT DIRECTLY BY A COMBINATION OF THE METER AND THE SCALE FACTOR AS SET BY DS11, 12 & 13. DS11 IS ENERGIZED FOR MILLIGERTZ, DS12 FOR HERTZ, AND DS13 FOR KILOHERTZ.

THE METER BECOMES DIRECT READING FREQUENCY WITH FREQUENCY RANGE SETTING DECIMAL POINT AUTOMATICALLY.

2.1.7 - POWER -

S18, DS14, POWER SWITCH AND LIGHT -

S18 TURNS POWER ON WHEN DEPRESSED. DS14 IS ENERGIZED BY POWER 'ON'.

2.1.8 - 916XH FRONT PANEL

THE 916XH OPERATES AT TEN TIMES THE FREQUENCY OF THE 916. S1 SETS 1 HZ, 10 HZ, 100 HZ, 1 KHZ, 10 KHZ AND 100 KHZ AS FULL SCALE.

R1 SETS THE FRACTION OF FULL SCALE.

THUS, TO SET 25 HZ, PUT S1 ON 100 HZ FULL SCALE, AND R1 ON 0.250.

M2 READOUT OF FREQUENCY IS DIRECT READING.

S2, R2 OPERATE THE SAME AS S1, R1 FOR STOP FREQUENCY SETTING.

THE METER READOUT OF FREQUENCY IS DIRECT READING.

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916XH

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL

REFERENCE: DRAWING NO. C102927-1, SH. 5

2.2.1 - ASSEMBLY - A1 -

THIS PANEL PROVIDES BNC'S FOR ALL OF THE CONNECTIONS TO THE ITEM UNDER TEST, AND FOR THE SIGNALS TO THE X-Y,Y PLOTTER. IT ALSO PROVIDES FOR CALIBRATION OF THE PLOTTER BY SWITCHES THAT INSERT CALIBRATE LEVELS.

J1B, J2B - CH#1 '+' & '-' INPUTS -

IN PARALLEL WITH J1A & J2A ON FRONT PANEL. (IF SINGLE ENDED RETURN SIGNAL IS USED, THE UNUSED INPUT MUST BE GROUNDED).

J3B, J4B - CH#2 '+' & '-' INPUTS -

IN PARALLEL WITH J3A AND J4A ON FRONT PANEL. (IF SINGLE ENDED RETURN SIGNAL IS USED, THE UNUSED INPUT MUST BE GROUNDED).

J5B - OUTPUT -

IN PARALLEL WITH J5A ON FRONT PANEL. TEST SIGNAL TO ITEM UNDER TEST.

J6 - A.R. 2/1 -

AMPLITUDE RATIO CH#2/CH#1 IN DB AT 2.0 VOLT/20DB. ZERO VOLT = RATIO OF 1/1. SEE S-22.

J7 - AMP - 1 -

AMPLITUDE CH#1 IN DB (OF FUNDAMENTAL)

+2.0 VOLT = +20. DB = 10 VOLT PEAK;
ZERO VOLT = ZERO DB = 1.0 VOLT PEAK;
-2.0 VOLT = -20 DB = 0.1 VOLT PEAK.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL - CONT'D.

2.2.1 - ASSEMBLY - A1

J8 - PHASE

PHASE SHIFT (CH#2 - CH#1) IN DEGREES. ±1.80 VOLT = ±180.0 DEGREES. SEE SW23.

J9 - AMP 2

AMPLITUDE CH#2 IN DB (OF FUNDAMENTAL). SCALED AS FOR AMP 1, J7 ABOVE.

J10 - LIN, LOG FREQUENCY AS SELECTED BY SW24

LOG FREQUENCY - 2.0 VOLT/DECADE.

ZERO VOLT = 10.00 HZ; -2.0 VOLT = 1.00 HZ; +4.0 VOLT = 1000 HZ., ETC.

LIN FREQUENCY - REPEATS IN EACH FREQUENCY RANGE.

+10.0 VOLT FULL SCALE. LINEAR AND DIRECT READING; EXAMPLE - 4.00 VOLT = .4 OF FULL SCALE. IF FREQUENCY RANGE IS 1.0 HZ FULL SCALE, FREQUENCY = .4 HZ, IF FREQUENCY RANGE IS 100 HZ FULL SCALE, FREQUENCY = 40. HZ.

SW20 - AGC 'IN' - 10 VOLT F.S.

THIS IS A MOMENTARY SWITCH. WHEN HELD IN THE DOWN POSITION, THE AGC SYSTEM IS TURNED 'OFF' AND A '10 VOLT FULL SCALE' SENSITIVITY IS PRESENT.

SW20 IS ONLY USED IN 'FAST CALIBRATE' TO CHECK MULTIPLIER ZERO AND INTEGRATOR DRIFT.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL - CONT'D.

2.2.1 - ASSEMBLY - A1

S21 - SWP - 'IN-CAL'

THIS IS A MOMENTARY SWITCH. WHEN HELD DOWN IN THE 'CAL' POSITION, THE OPERATING FREQUENCY IN 'RESET' FREQUENCY IS DETERMINED BY R42 ON BOARD #2. IT SHOULD BE 10.0% OF FULL SCALE.

THE SWEEP WILL STOP ON THE SAME FREQUENCY RANGE AT THE FREQUENCY SET BY R52 OF BOARD #2. IT SHOULD BE 100.0% OF FULL SCALE.

S21 IS ONLY USED FOR RECALIBRATION OF THE SWEEP SYSTEM.

S22 - A.R. - +40 DB, -40 DB

S22 IS A TRIPLE THROW SWITCH WITH DUAL MOMENTARY ACTION. IT IS USED TO CALIBRATE THE AMPLITUDE RATIO PLOT. WHEN HELD IN THE DOWN (+40 DB) POSITION, +4.0 VOLTS APPEARS AT J6B (& J101-2). THE PLOTTER SENSITIVITY IS SET FOR +40.0 DB. SIMILARLY, WHEN HELD IN THE UP (-40 DB) POSITION, -4.0 VOLTS APPEARS AT J6B (& J101-2). IT IS USED TO CHECK AND SET PLOTTER SENSITIVITY.

S22 RETURNS TO ITS CENTER POSITION (M-MEASURE) FOR NORMAL OPERATION OF THE PLOTTER FROM THE ANALYZER OUTPUT.

S23 - PHASE +90°, -180°

S23 IS A TRIPLE THROW SWITCH WITH DUAL MOMENTARY ACTION. IT IS USED TO CALIBRATE THE PHASE PLOT. WHEN HELD IN THE UP POSITION, +.90 VOLTS APPEARS AT J8B (& J102-1). THE PLOTTER SENSITIVITY IS SET FOR +90°. SIMILARLY, WHEN HELD IN THE 'DOWN' POSITION, (-180 DEGREES), -1.80 VOLTS IS CONNECTED TO J8B (& J102-1). IT IS USED TO CHECK AND SET PLOTTER SENSITIVITY.

S23 RETURNS TO ITS CENTER POSITION (M-MEASURE) FOR NORMAL OPERATION OF THE PLOTTER FROM THE ANALYZER OUTPUT.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL - CONT'D.

2.2.1 - ASSEMBLY - A1

SW24 - LOG-LIN

SW24 IS A TWO POSITION SWITCH WHICH DETERMINES WHETHER THE DC VOLTAGE PROPORTIONAL TO LOG FREQUENCY OVER THE ENTIRE 6 1/2 DECADE FREQUENCY RANGE, OR THE DC VOLTAGE LINEARLY PROPORTIONAL TO FREQUENCY WITHIN A FREQUENCY RANGE IS CONNECTED TO J10.

SEE J10 ABOVE FOR SCALING.

USE SW24 IN 'LOG' FOR ALL MULTI-DECADE SWEEPS AND PLOT.

2 - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL - CONT'D.

2.2.2 - ASSEMBLY - A2 -

J102 - READOUT ANALOG (& REMOTE CONTROL LINES)

J102 CARRIES THE ANALOG READOUTS AND SUCH REMOTE CONTROL POINTS AS WILL BE USEFUL IN CALIBRATION, AND FOR A LIMITED REMOTE PROGRAM CAPABILITY (OR INTERLOCK TO A TEST SETUP).

J102-1 - PHASE SHIFT

DC VOLTAGE PROPORTIONAL TO PHASE SHIFT AND SCALED ±1.80 VOLTS = ±180°. CALIBRATE LEVELS ARE GENERATED BY S23 AS +90°, -180° HELD IN 'UP' OR 'DOWN' POSITION.

J102-2 - AMPLITUDE RATIO (DB)

DC VOLTAGE PROPORTIONAL TO AMPLITUDE RATIO IN DB, AND SCALED 2.0 VOLTS = 20 DB. ZERO VOLTS - ZERO DB - 1/1 IN AMPLITUDE. CALIBRATE LEVELS ARE SUBSTITUTED FOR A.R. BY SW22 AS +40 DB (+4.0 VOLTS) WHEN S22 IS HELD IN 'DOWN' POSITION, OR AS -40 DB (-4.0 VOLTS) WHEN S22 IS HELD IN 'UP' POSITION.

J102-3 - AMP CH1 - DB

DC VOLTAGE PROPORTIONAL TO AMPLITUDE (OF FUNDAMENTAL) OF CH1 IN DB, 2.0 VOLT/20 DB; ZERO VOLTS = 1.0 VOLT PEAK; +2.0 VOLT = 10.0 VOLT PEAK, ETC.

J102-4 - AMP CH2 IN DB

SAME AS J102-3 FOR CH #2.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL - CONT'D.

2.2.2 - ASSEMBLY - A2

J102-5 - LIN FREQUENCY (DCS1)

DC VOLTAGE LINEARLY PROPORTIONAL TO FREQUENCY WITHIN THE FREQUENCY RANGE. +10.0 VOLTS = FULL SCALE. +1.00 VOLT = 0.1 OF FULL SCALE. REPEATS FOR EACH FREQUENCY RANGE. REFERRED TO AS DCS1.

J102-6 - LOG FREQUENCY

DC VOLTAGE PROPORTIONAL TO LOG FREQUENCY OVER 6 1/2 DECADE RANGE OF 916, SCALED FOR 2.0 VOLT/DECADE. ZERO VOLTS AT 1.00 HZ; +2.0 VOLTS = 10 HZ; -4.0 VOLTS = .010 HZ, ETC.

102-7 - GROUND

J102-8 - $\overline{\text{FLAG}}$

NORMALLY AT -15 VOLTS. GOES TO NEAR GROUND WHEN:

THERE IS AN UNDERLOAD OR OVERLOAD IN EITHER CHANNEL OF THE 916; OR WHEN NEW RESULTS ARE BEING ENTERED INTO THE OUTPUT (EOC PERIOD).

J102-9 - SWEEP STOP -

LOGIC LEVEL GOES FROM -15 VOLTS TO NEAR GROUND WHEN SWEEP FREQUENCY REACHES STOP FREQUENCY SETTING.

THE REMAINING PINS ARE PRIMARILY REMOTE CONTROL POINTS.

J102-10 - 'OFF'

GROUNDING J102-10 TURNS 'OFF' THE 916 ANALYZER (AND TEST SIGNAL GENERATOR), IN THE SAME MANNER AS S5 ON THE FRONT PANEL. THIS POINT IS NORMALLY AT -15 VOLTS.

IF S5 IS 'OFF', J102-10 CANNOT BE USED TO TURN IT 'ON'.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL

2.2.2 - ASSEMBLY - A2 -

J102-11 - $\overline{X5}$ INTEGRATE

CONNECT THIS PIN TO -15 VOLTS (AS TO J102-23), WILL CAUSE THE ANALYZER TO GO FROM 'X5' OUT TO 'X5' IN. IF THE FRONT PANEL 'S15' IS SET FOR 'X5 IN', J102-11 CANNOT CHANGE IT TO 'X5 OUT'.

J102-12 - AGC TO 10V FULL SCALE

GROUNDING J102-12 REMOVES THE AGC FROM OPERATION AND LEAVES BOTH CHANNELS AT 10 VOLT FULL SCALE SENSITIVITY. THIS IS USED AS PART OF 916 FAST CALIBRATE PROCEDURE. IT IS IDENTICAL TO HOLDING SW20 IN THE DOWN POSITION.

J102-12 RETURNS TO NEAR -15 VOLTS WHEN NOT IN USE.

J102-13 - SWEEP ONE FREQUENCY RANGE

CONNECT -15 VOLTS TO J102-13 AND THE SWEEP WILL NOT SWITCH FROM THE START FREQUENCY RANGE TO THE NEXT ONE. THIS IS USED TO CALIBRATE THE SWITCHING POINT (R52 ON BD#2).

REMOVE -15 VOLTS FOR PROPER SWEEP SYSTEM OPERATION.

SW21 HELD IN THE DOWN POSITION DOES THE SAME THING.

J102-14 - FILTER

GROUND J102-14 TO TURN ON THE INPUT FILTER. THIS IS IDENTICAL TO OPERATION OF S13 ON FRONT PANEL.

IF S13 IS AT 'FILTER IN' POSITION, J102-14 HAS NO EFFECT.

J102-15 - SWEEP CALIBRATE - START

GROUNDING J102-15 WITH SWEEP MODE IN RESET (S9A), PUTS THE FREQUENCY AT 10.0% OF FULL RANGE AS DETERMINED BY R42 ON BD#2.

THIS IS USED TO CALIBRATE THE START OF SWEEP IN EACH NEW FREQUENCY RANGE. IT IS NOT USED IN NORMAL OPERATION.

S21 ALSO PERFORMS THIS FUNCTION WHEN HELD IN THE DOWN POSITION.

J102-16 - PRESET GAIN

GROUNDING J102-16 SETS THE CH#1 & CH#2 FULL SCALE SENSITIVITY 40 MV F.S. IT IS USED EXACTLY AS S10 ON FRONT PANEL TO EXPEDITE THE AGC ATTAINING THE CORRECT GAIN. THE GROUND MUST BE REMOVED (POINT WILL GO TO -15 VOLTS) FOR THE AGC TO FUNCTION.

J102-17 - 'HOLD SWEEP'

CONNECT J102-17 TO -15 VOLTS TO PUT SWEEP IN 'HOLD' DURING A SWEEP. OPERATION IS THE SAME AS S9C ON FRONT PANEL. DO NOT USE THIS POINT UNLESS ANALYZER IS OUT OF RESET AND INTO SWEEP.

IF IN 'HOLD', (DUE TO S9C), THIS PIN CANNOT REMOVE THE 'HOLD'.

J102-18 - 'ANALYSIS RESET'

CONNECT THIS PIN TO -15 VOLTS AND THE 916 WILL COMPLETE THE CYCLE-OF-ANALYSIS NOW IN PROGRESS. IT WILL NOT START A NEW CYCLE OF ANALYSIS UNTIL THE -15 VOLTS IS REMOVED.

THE TEST SIGNAL GENERATOR WILL CONTINUE TO OPERATE IN A NORMAL FASHION.

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL -

2.2.2 - ASSEMBLY - A2 -

J102-19 - A.G.C. - STOP

-15 VOLTS APPLIED TO THIS PIN WILL STOP THE A.G.C.'S RESPONSE TO SIGNAL OVERLOAD OR SIGNAL UNDERLOAD CONDITIONS. IT WILL NOT PREVENT NOISE OVERLOAD FROM CAUSING A GAIN CHANGE.

J102-20 - A.G.C. - STOP

-15 VOLTS APPLIED TO THIS PIN WILL STOP THE A.G.C.'S RESPONSE TO NOISE OVERLOAD. IT WILL NOT PREVENT SIGNAL OVERLOAD AND UNDERLOAD FROM CAUSING A GAIN CHANGE.

J102-21 - SPARE

J102-22 - SPARE

J102-23 - -15 VOLTS FOR ABOVE.

J102-24- GROUND

IN USING J102-10 THRU 20 BE CAREFUL TO ALLOW POINTS TO RETURN TO GROUND OR TO -15 VOLTS AFTER REMOVING OPERATE INPUT OF -15 VOLTS OR GROUND.

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916XH

2. - FRONT & REAR PANEL CONTROLS, BNC'S, CONNECTORS & READOUTS

2.2 - REAR PANEL

2.2.3 - AUTOMATIC PEN LIFT

REFERENCE: DRAWING NO. B104102
REMOTE CONNECTOR - J105

SWEEP, RESET, OSCILLATOR RESET AND $\overline{\text{END}}$ OF SWEEP COMMAND (STOP SIGNAL) WILL DEENERGIZE RELAY K1. DURING SWEEP, K1 IS ENERGIZED.

J105 - PINS 1 & 5 ARE CLOSED DURING SWEEP.

J105 - PINS 1 & 3 ARE CLOSED DURING SWEEP RESET, OSCILLATOR RESET AND END OF SWEEP (STOP).

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916 XH

3. - OPERATION

3.1 - POWER

CONNECT POWER LINE TO J20 ON REAR PANEL.

DEPRESS POWER SWITCH (S18) AND OBSERVE LIGHT (DS14) GO ON.

3.2 - CONNECTION OF TEST SIGNAL TO ITEM-UNDER-TEST

THE TEST SIGNAL IS CONNECTED FROM J5A ON THE FRONT PANEL, OR J5B ON THE REAR PANEL, AS THE INPUT TO THE ITEM-UNDER-TEST.

IT IS USUALLY BEST TO SET THE TEST SIGNAL 'OFFSET', AMPLITUDE, AND FREQUENCY BEFORE CONNECTING. SEE SECTION 3.3 BELOW.

IF DESIRED, PUT S5 'OFF' (TEST SIGNAL 'OFF'), AND S8 ON '0' FOR ZERO TEST SIGNAL AND ZERO OFFSET TO START.

3.3 - SETUP OF TEST SIGNAL

3.3.1 - FREQUENCY

PUT SWEEP IN 'RESET' (S19A).
USE S1, R1 TO SET TEST FREQUENCY.

EXAMPLE: 1.25 HZ DEPRESS S1B - 10 HZ FULL SCALE.
SET R1 ON .125.

3.3.2 - AMPLITUDE

USE VOLTS F.S. CONTROLS S7, R3 TO SET PEAK VALUE OF TEST SIGNAL.

EXAMPLE: PEAK VALUE OF .75 VOLTS.
DEPRESS S7B (1VOLT PEAK) AND SET R3 ON .750.

3.3.3 - WAVESHAPE

USE S6 TO SELECT OUTPUT WAVESHAPE (SINE, TRIANGLE, SQUARE WAVE).

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3. - OPERATION

3.3 - SETUP OF TEST SIGNAL

3.3.4 - OFFSET

USE S8 AND R4 TO ESTABLISH POLARITY AND AMPLITUDE OF OFFSET. READ OFFSET ON M1 WITH S16D DEPRESSED. (PUT S5 IN 'OFF').

3.3.5 - TURN ON OF TEST SIGNAL

PUT S5 'ON'. TEST SIGNAL APPEARS ON BNC 'J5'.

3.4 - RETURN SIGNAL CONNECTION & SETUP

3.4.1 - CONNECTION

CONNECT THE CH#2 TEST SIGNAL TO 'J1A & J2A' ON FRONT PANEL, OR 'J1B & J2B' ON REAR PANEL.

CONNECT THE CH#1 TEST SIGNAL TO 'J3A & J4A' ON THE FRONT PANEL, OR 'J3B & J4B' ON THE REAR PANEL.

IF A SINGLE ENDED RETURN SIGNAL IS USED, SHORT THE UNUSED BNC TO GROUND.

3.4.2 - 'PRESET GAIN'

DEPRESS 'PRESET GAIN' ONCE. RELEASE THE ANALYZER (S5 IN 'OFF'). WATCH THE OVERLOAD (DS7 IN CH#2, DS5 IN CH#1) AND UNDERLOAD (DS6, DS5) LIGHTS. WHEN ALL FOUR ARE DEENERGIZED, THE ANALYZER'S A.G.C. HAS SETTLED OUT AND THE RESULTS CAN BE READ OUT ON M1 AND M2.

3.4.3 - 'FAST DC REJECT'

IF A LARGE DC OFFSET WAS PRESENT ON A RETURN SIGNAL, DEPRESS THAT CHANNEL'S 'FAST DC REJECT' SWITCH (S12 & S11) FOR A SHORT TIME (TO RAPIDLY CHARGE INPUT CAPACITORS TO INPUT DC OFFSET).

3.4.4 - FILTER IN-OUT

IF LARGE NOISE COMPONENTS ABOVE 1000 HZ ARE PRESENT, ACTUATE 'FILTER IN' SWITCH (S13).

3.4.5 - UNDERLOAD LIGHT REMAINS 'ON'

IF THE UNDERLOAD LIGHT IN EITHER (OR BOTH) CHANNEL REMAINS 'ON', THE FUNDAMENTAL COMPONENT OF THE RETURN SIGNAL IS UNDER 2.5 MV. CONSIDER ADDING A PREAMPLIFIER BETWEEN THE TEST POINT AND THE MODEL 916 FREQUENCY RESPONSE ANALYZER.

3.5 - FREQUENCY BY FREQUENCY TESTING

3.5.1 - INTRODUCTION

THE BELOW STEPS ARE SUFFICIENT FOR FREQUENCY BY FREQUENCY TESTING.

CHECK SWEEP IN RESET (S9A).

USE S5 TO START AND STOP TEST.

USE E.O.C. LIGHT (DS10) TO CHECK ANALYSIS CYCLES FOLLOWING ONE ANOTHER AT REGULAR TIME INTERVALS.

3.5.2 - 'X5' INTEGRATE - NOISE REJECTION

READ M1 & M2 FOR AMP RATIO (DB) AND PHASE SHIFT. THE VARIATION IN THE RESULTS FROM READING-TO-READING IS A MEASURE OF THE 'NOISE' RESPONSE OF THE ANALYZER. USE 'X5' INTEGRATE 'IN' (S15) TO DECREASE THE BOUNCE, IF NECESSARY. OF COURSE, THE TIME BETWEEN READINGS INCREASES.

3. - OPERATION

3.6 - SWEEP

3.6.1 - CONNECTIONS TO PLOTTER

CONNECT LOG FREQUENCY (J102-6 OR J10 WITH S24 IN LOG) TO THE 'X' AXIS OF PLOTTER.

CONNECT AMP RATIO (DB) (J6 OR J102-2) TO THE 'Y', AXIS OF PLOTTER.

CONNECT PHASE SHIFT (DEGREES) (J8 OR J102-1) TO THE Y_2 AXIS OF PLOTTER.

3.6.2 - CALIBRATION OF PLOTTER

'X' AXIS - FREQUENCY

THE LOG FREQUENCY SIGNAL OF THE 916 HAS ZERO VOLTS FOR 10.00 HZ. THEREFORE, SET ZERO INPUT OF 'X' AXIS TO 10.00 HZ ON PLOT USING ZERO ADJUST ON PLOTTER.

PUT ANALYZER AT 100 HZ, OR 1.0 HZ (USE 10/1 CHANGES IN FREQUENCY WITH S1) AND SET 'X' AXIS SPAN. RECHECK ZERO AND SPAN.

'Y' AXIS - AMP RATIO

AMP RATIO OF 1/1 IS ZERO VOLTS OUT OF 916. USE PLOTTER Y_1 ZERO ADJUST TO SET ZERO DB POINT. TWO VOLTS/20 DB IS 916 SCALE FACTOR. USE Y_1 AXIS ON 1 VOLT/IN IF 10 DB/IN IS SUITABLE, ETC.

IF A SPECIAL SCALING IS REQUIRED, HOLD S22 (ON REAR PANEL) UP TO INJECT '-40 DB' CALIBRATION POINT; OR HOLD S22 DOWN TO INJECT +40 DB CALIBRATION POINT AND USE PLOTTER Y_1 SPAN ADJUST. RECHECK Y_1 ZERO AND Y_1 SPAN.

3. - OPERATION

3.6 - SWEEP - CONT'D.

3.6.2 - CALIBRATION OF PLOTTER

'Y_2' AXIS - PHASE SHIFT

ZERO PHASE IS ZERO VOLTS ON MODEL 916 OUTPUT. SET DESIRED ZERO PHASE POINT ON PLOTTER USING 'Y_2' ZERO ADJUST.

±1.80 VOLTS IS ±180° ON MODEL 916 OUTPUT. SET FIXED GAIN OF 1 VOLT/IN FOR 1.80V = 180°, ETC.

IF NON-STANDARD SPAN IS DESIRED, USE SW23 ON REAR PANEL HELD IN UP POSITION TO INJECT +90°. ADJUST Y_2 SPAN FOR DESIRED 90° PLOT. HOLD SW23 DOWN, TO INJECT -180° PHASE. CHECK Y_2 SPAN. RECHECK ZERO.

3.6.3 - SWEEP

3.6.3.1 - STARTING CONDITION

AFTER CALIBRATING THE PLOTTER, SETTING THE TEST SIGNAL AMPLITUDE, WAVESHAPE AND START FREQUENCY AND ALLOWING THE 916 FREQUENCY RESPONSE ANALYZER TO SOLVE FOR CH#2/CH#1 AS DESCRIBED ABOVE FOR SINGLE FREQUENCY MEASUREMENTS, THE OPERATOR IS READY TO SET THE SWEEP CONDITIONS, AS FOLLOWS:

3.6.3.2 - STOP FREQUENCY

USE S2 TO SET THE STOP FREQUENCY RANGE, AND R2 TO SET THE STOP FREQUENCY WITH THE RANGE. (STOP FREQUENCY MUST EXCEED START FREQUENCY).

3.6.3.3 - SWEEP SPEED

USE S3 AND S4 TO SET THE SWEEP SPEED. THIS SPEED MAY BE ALTERED AS THE SWEEP PROCEEDS. A GOOD STARTING POINT (ABOVE 0.1 HZ) IS N = 3 (S3), X.6 (S4). SLOW THE SWEEP IF THE FREQUENCY RESOLUTION IS NOT SUFFICIENT OR IF GOING THRU A RESONANCE. SPEED UP THE SWEEP, IF THE NUMBER OF NEW READINGS IS EXCESSIVE FOR THE CHANGES OCCURRING IN THE FREQUENCY RESPONSE.

3. - OPERATION

3.6 - SWEEP - CONT'D.

3.6.3 - SWEEP

3.6.3.4 - SWEEP CONTROL

S9 IS USED FOR SWEEP CONTROL. DEPRESS S9B AND THE SWEEP BEGINS. DS2 IS ENERGIZED INDICATING THE ANALYZER IS IN SWEEP.

THE SWEEP CONTINUES TO THE STOP FREQUENCY UNLESS THE OPERATOR PUTS SWEEP INTO HOLD (S9C) (HE MAY THEN RETURN TO 'SWEEP' AND CONTINUE TO THE 'STOP' FREQUENCY), OR TURNS THE SIGNAL 'OFF' WITH S5 (SWEEP IN HOLD). (IT WILL CONTINUE IF S5 IS RETURNED TO 'ON'). DS3 IS 'ON' WHEN IN 'HOLD'.

AT THE STOP FREQUENCY, 'DS2' GOES OFF, AND DS9 IS ENERGIZED. THE TEST SIGNAL IS TURNED OFF AND THE HOLD LIGHT (DS3) GOES ON.

DURING SWEEP, THE OPERATOR MAY REVERSE THE SWEEP SENSE FROM INCREASING FREQUENCY TO DECREASING FREQUENCY BY HOLDING S14 DOWN. THIS MAY BE USED TO RETRACE A SMALL SEGMENT OF THE SWEEP BUT IT CANNOT BE USED TO SWITCH DOWN A FREQUENCY RANGE.

3 - OPERATION

3.7 - RECOMMENDED '916XH' CONNECTIONS TO ITEM UNDER TEST

FIG. 3-1 SHOWS THE RECOMMENDED CONNECTION OF THE MODEL 916XH TO THE ITEM UNDER TEST. THIS RECOMMENDATION IS PARTICULARLY IMPORTANT IN THE HIGHEST FREQUENCY RANGE.

THE TEST SIGNAL IS BROUGHT OUT TO DRIVE THE INPUT USING BOTH THE HIGH AND GROUND LEADS FROM THE 916 OUTPUT.

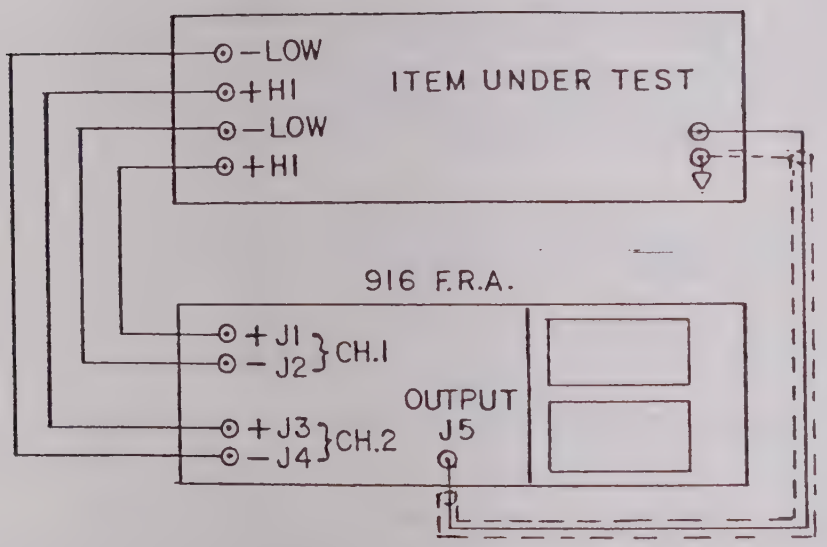
THE '+' AND '-' INPUTS TO EACH CHANNEL ARE CONNECTED TO THE HIGH AND LOW END OF THE LOCATION OF THE RETURN SIGNAL. (THIS PROVIDES FOR SOME COMMON MODE REJECTION OF THE VOLTAGE WHICH WILL DEVELOP BETWEEN THE TEST SIGNAL GROUND AND THE RETURN SIGNAL GROUND).

THESE PROCEDURES ARE MOST IMPORTANT IN THE HIGHEST FREQUENCY RANGE, AND WHEN MEASURING LOW AMPLITUDE SIGNALS (UNDER 10 MV).

IF A QUESTION ARISES CONCERNING THIS MATTER, CONTACT BAFCO, INC.

THE '+' AND '-' CONNECTIONS MAY BE REVERSED TO MOVE THE PHASE SHIFT 180° AT THE START OF THE PLOT.

NO	DESCRIPTION
A	RELEASE



RETURN SIGNALS

USE THE '+' AND '-' INPUT TO CONNECT TO HIGH AND LOW ENDS OF THE RETURN SIGNAL. EVEN IF LOW END IS GROUND, USE '-' INPUT TO REJECT VOLTAGE DROPS IN GROUND LINES.

FIG. 3-1

UNLESS OTHERWISE SPECIFIED FRACTIONS ± .015 TWO PL. DEC. ± .010 THREE PL. DEC. ± .005 ANGLES ±1/2 DEG. SURF. FIN. 125 MICROINCH	THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	BAFCO, INC.
916XH CONNECTION TO ITEM UNDER TEST	BY Grassi DATE 8-27-76 APPD DATE	A

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4. - THEORY OF OPERATION

4.1 - INTRODUCTION

TO APPRECIATE THE NOISE AND HARMONIC REJECTION CAPABILITIES OF THE MODEL 916, IT IS NECESSARY TO UNDERSTAND THE FOURIER INTEGRAL SIGNAL ANALYSIS METHOD AS APPLIED TO THE EXTRACTION OF A FUNDAMENTAL FROM SIGNAL PLUS NOISE PLUS HARMONICS (DISTORTION). SECTION 4.2 IS DEVOTED TO THE 'FOURIER INTEGRAL' AS APPLIED IN THE MODEL 916.

THE OVERALL OPERATION OF THE MODEL 916 IS PRESENTED IN SECTION 4.3 USING THE BLOCK DIAGRAM OF FIGURE 4-3.

THE INDIVIDUAL BLOCKS OF THE MODEL 916 ARE PRESENTED IN GREATER DETAIL, AS FOLLOWS:

SECTION 4.4 - TEST AND REFERENCE SIGNAL GENERATION AND EXTENDED SWEEP.

SECTION 4.5 - RETURN SIGNAL FOURIER ANALYZERS, INCLUDING INPUT PREAMPLFIER AND AMPLIFIER.

SECTION 4.6 - TIMING SYSTEM.

SECTION 4.7 - PHASE SHIFT, AMPLITUDE AND AMPLITUDE RATIO, (DB) COMPUTERS.

SECTION 4.8 - AUTOMATIC GAIN CONTROL SYSTEM.

SECTION 4.9 - ENGINEERING UNITS -
THE ATTENUATOR SYSTEM AND 'X5-IN, OUT' INTEGRATE CONSTANT.

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916XH

4.2 - HARMONIC & NOISE REJECTION

4.2.1 - FOURIER INTEGRAL ANALYSIS

THE FOURIER INTEGRAL AS USED IN THE MODEL 916 IS:

$$\text{OUTPUT}_1 = \frac{1}{T}\int_0^T f(t)\,\sin\omega_0 t.dt \qquad (4.2\text{-}1)$$

$$\text{OUTPUT}_2 = \frac{1}{T}\int_0^T f(t)\,\cos\omega_0 t.dt \qquad (4.2\text{-}2)$$

WHERE:

f(t) IS THE OUTPUT OF THE INPUT AMPLIFIER (RETURN SIGNAL AFTER PASSING THROUGH THE INPUT PREAMPLIFIER AND INPUT AMPLIFIER).

T = INTEGRATION TIME

ω_0 = TEST FREQUENCY IN RAD/SEC.

NORMALLY THE INTEGRATION TIME IS A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY OR -

$$T = \frac{2\pi}{\omega_0} N \qquad (4.2\text{-}3)$$

WHERE: N = NUMBER OF CYCLES OF TEST FREQUENCY OVER WHICH THE INTEGRATION TAKES PLACE (INTEGER)

AS SHOWN IN FIG. 4.5-1, EQS. 4.2-1, AND 4.2-2 ARE THE OPERATIONS PERFORMED ON BOARDS #7 AND #8 FOR RETURN SIGNALS OF CH#1 AND CH#2, RESPECTIVELY.

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FOR THE PURPOSES OF EVALUATING THE EFFECT OF FOURIER INTEGRAL ANALYSIS, f(t) IS EXPANDED INTO ITS EQUIVALENT FOURIER SERIES AS

$$f(t) = A_0 + A_1 \text{ SIN } \omega_1 t + A_2 + \text{----} A_n \text{ SIN } n\omega_1 t$$

$$+ B_1 \text{ COS } \omega_1 t + B_2 \text{ COS } 2\omega_1 t + \text{----} B_n \text{COS } n\omega_1 t$$

$$+ \text{NOISE} \qquad (4.2\text{-}4)$$

WHERE

A_0 = D.C. TERM

A_1 = AMPLITUDE OF IN-PHASE COMPONENT OF FUNDAMENTAL

A_2 = AMPLITUDE OF IN-PHASE COMPONENT OF 2ND HARMONIC

A_n = AMPLITUDE OF IN-PHASE COMPONENT OF nTH HARMONIC

B_n = SAME AS 'A_n' FOR QUADRATURE COMPONENT OF nTH HARMONIC

NOISE = NON HARMONICALLY RELATED COMPONENTS OF f(t).

NORMALLY, HARMONIC CONTENT IS DISTORTION IN THE WAVESHAPE DUE TO NON-LINEARITIES IN THE SYSTEM.

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4.2.2 - HARMONIC REJECTION

CONSIDER EQ. 4.2-1, AND EQ. 4.2-2 FOR THE HARMONIC TERMS IN f(t) (EG. 4.2-4)

$$\frac{A_n}{T}\int_0^T \text{SIN}\,\omega_1 t \cdot \text{SIN}\, n\omega_1 t \cdot dt = 0 \qquad (4.2\text{-}5)$$

FOR $n \neq 1$, $\quad T = \frac{2\pi}{\omega_1} N$

$$\frac{B_n}{T}\int_0^T \text{SIN}\,\omega_1 t \cdot \text{COS}\, n\omega_1 t \cdot dt = 0 \qquad (4.2\text{-}6)$$

FOR ALL 'n' $\quad T = \frac{2\pi}{\omega_1} N$

$$\frac{B_n}{T}\int_0^T \text{COS}\,\omega_1 t \cdot \text{COS}\, n\omega_1 t \cdot dt = 0 \qquad (4.2\text{-}7)$$

FOR $n \neq 1$

$$\frac{A_n}{T}\int_0^T \text{COS}\,\omega_1 t \cdot \text{SIN}\, n\omega_1 t \cdot dt = 0 \qquad (4.2\text{-}8)$$

FOR all 'n'

OR (IN WORDS) -

THE FOURIER INTEGRAL CARRIED OUT FOR A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY REJECTS ALL HARMONICS OF THE TEST FREQUENCY; AND THE (EQ. 4.2-1) IN-PHASE TERM REJECTS THE QUADRATURE COMPONENT OF THE FUNDAMENTAL (EQ. 4.2-6 FOR n = 0'S), THE (EQ. 4.2-2) QUADRATURE TERM REJECTS THE IN-PHASE COMPONENT OF THE FUNDAMENTAL (EQ. 4.2-8) FOR n = 1). THE REJECTION IS PERFECT IF THE MULTIPLICATION IS EXACT, AND IF THE REFERENCE SIGNAL IS LOW IN DISTORTION.

THE MODEL 916 ACHIEVES MORE THAN 46 DB REJECTION OF HARMONICS.

THE FUNDAMENTAL TERMS ARE DETERMINED BY THE FOURIER INTEGRAL ANALYSIS AS

$$\frac{A_1}{T}\int_0^T \text{SIN}\,\omega_1 t \cdot \text{SIN}\,\omega_1 t \cdot dt = \frac{A_1}{2} \qquad (4.2\text{-}9)$$

$$\frac{B_1}{T}\int_0^T \text{COS}\,\omega_1 t \cdot \text{COS}\,\omega_1 t \cdot dt = \frac{B_1}{2} \qquad (4.2\text{-}10)$$

OR, EQS. 4.2-1, & 4.2-2 DETERMINE THE IN-PHASE (A_1) AND QUADRATURE (B_1) COMPONENT OF THE FUNDAMENTAL FREQUENCY.

THUS, FOURIER INTEGRAL ANALYSIS AUTOMATICALLY AND COHERENTLY SEPARATES THE FUNDAMENTAL FROM THE HARMONICS PRESENT IN THE RETURN SIGNAL. (IT MEASURES THE TRUE 'DESCRIBING FUNCTION' OF THE RETURN SIGNAL).

4.2.3 - NOISE REJECTION

NOISE IS DEFINED AS RETURN SIGNAL FREQUENCY CONTENT WHICH IS NOT HARMONICALLY RELATED TO THE TEST SIGNAL. THIS INCLUDES BOTH WIDE BAND NOISE, AND SINGLE FREQUENCY COMPONENTS SUCH AS LINE NOISE, CARRIER FREQUENCY, DITHER SIGNAL, ETC.

SOLVING THE EQUATIONS 4.2-1 AND 4.2-2 FOR THEIR RESPONSE TO NOISE, ONE OBTAINS A WORSE CASE RESULT OF -

$$\text{AMPLITUDE} = \frac{2\pi}{N} \cdot \frac{\omega/\omega_0}{[1 + \omega/\omega_0]} \cdot \frac{\text{SIN}\left[N\pi \frac{\omega}{\omega_0}\right]}{[1 - \omega/\omega_0]} \quad \text{(4.2-11)}$$

FIG. 4.2-1 IS A PLOT OF EQ. 4.2-11 FOR N = 1, 2, 20 CYCLES OF THE TEST FREQUENCY.

TO FULLY APPRECIATE THE SIGNIFICANCE OF THESE CURVES AND OF EQ. 4.2-11, THE FOLLOWING FACTORS MUST BE UNDERSTOOD.

1. - NOISE REJECTION INCREASES AS 'N' - THE NUMBER OF CYCLES INTEGRATED OVER INCREASES. THIS IS A USUAL TRUISM IN NOISE REJECTION BY FILTERS. IT CAN BE GENERALIZED INTO, 'GREATER NOISE REJECTION REQUIRES LONGER ANALYSIS TIME.'

2. - THE RESULTS SHOWN IN FIG. 4.2-1 AND GIVEN BY EQ. 4.2-11 ARE 'WORST' CASE RESULTS. WHAT HAPPENS IN PRACTICE IS THE FOLLOWING:

   BROAD-BAND NOISE

   PERTURBATES THE RESULT IN A RANDOM FASHION, AND AT MUCH LESS AMPLITUDE THAN THE 'WORST CASE' WOULD APPEAR TO INDICATE. IN ANY CASE, THE '916' WILL IMMEDIATELY SHOW THE EFFECT OF THE BROAD BAND NOISE BY THE EXTENT OF THE VARIATION IN THE RESULTS (PHASE SHIFT AND AMPLITUDE RATIO) FROM ANALYSIS CYCLE TO ANALYSIS CYCLE. THE VARIATION CAN BE REDUCED BY USING 'X5 INTEGRATE' IN. THE OPERATOR CAN AVERAGE THE RESULTS AND OBTAIN THE EQUIVALENT OF STILL LONGER INTEGRATE TIMES.

SINGLE FREQUENCY NOISE COMPONENTS CAUSE A BEAT IN THE RESULTS AT THE DIFFERENCE FREQUENCY (TEST FREQUENCY-NOISE FREQUENCY). AGAIN, THE USE OF 'X5 INTEGRATE' IN, REDUCES THE FREQUENCY RANGE AROUND THE NOISE FREQUENCY AT WHICH A SIGNIFICANT UPSET IN THE RESULTS WILL OCCUR. THE PRESENCE OF THE BEAT REVEALS TO THE OPERATOR THAT A SINGLE FREQUENCY NOISE COMPONENT IS PRESENT (AND ITS FREQUENCY). AGAIN, THE OPERATOR CAN AVERAGE THE BEAT AND OBTAIN A GREATLY IMPROVED RESULT EQUIVALENT TO A STILL LONGER INTEGRATE TIME.

3. - MOST IMPORTANT OF ALL, IS THE FACT THAT NEITHER BROAD-BAND NOISE NOR SINGLE FREQUENCY NOISE PRODUCES A BIASED, INCORRECT RESULT.

ALL NOISE PERTURBATES THE RESULTS FROM ANALYSIS CYCLE TO ANALYSIS CYCLE. THE OPERATOR CAN ALWAYS IMPROVE HIS UNDERSTANDING OF THE SYSTEM PERFORMANCE BY MORE CLOSELY EXAMINING THE NOISE RESPONSE, BY INCREASING THE INTEGRATE TIME, AND BY ADDING INPUT (DUAL MATCHED FILTERS).

THE RESULTS OBTAINED BY THE 916 SHOULD NOT LEAD THE OPERATOR INTO BELIEVING THAT THE WRONG FREQUENCY RESPONSE IS PRESENT.

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4.3 - OVERALL OPERATION

FIGURE 4-3 IS A BLOCK DIAGRAM OF THE MODEL 916 SWEEP FREQUENCY RESPONSE ANALYZER. IT IS MADE UP OF FIVE MAJOR SUB-SYSTEMS.

THE REFERENCE AND TEST SIGNAL GENERATOR ESTABLISHES THE FREQUENCY OF OPERATION, SUPPLY 10 SINωt, AND 10 COSωt REFERENCE SIGNALS TO THE FOURIER INTEGRAL ANALYZER, AND SUPPLIES THE TEST SIGNAL TO THE ITEM UNDER TEST FROM AN ATTENUATED PORTION OF THE REFERENCE SIGNAL THRU A POWER AMPLIFIER.

THIS SECTION ALSO INCLUDES THE SWEEP SYSTEM WHICH LOGARITHMICALLY SWEEPS THE TEST SIGNAL FROM ANY 'START' TO ANY 'STOP' FREQUENCY. THE SWEEP IS CONTINUOUS.

THERE ARE TWO RETURN SIGNAL FOURIER INTEGRAL ANALYZERS. EACH RETURN SIGNAL IS OPERATED ON IN THE FOLLOWING SEQUENCE:

D.C. OFFSET IS REMOVED BY A MATCHED HIGH PASS INPUT FILTER. THE DOUBLE-ENDED RETURN SIGNAL IS CONVERTED TO SINGLE-ENDED.

THE SIGNAL IS AMPLIFIED FROM 1.0 TO 1,024 VOLTS/VOLT (AS SELECTED BY THE AUTOMATIC GAIN CONTROL SYSTEM). HIGH PASS FILTER ACTION SPEEDS UP D.C. AND LOW FREQUENCY REJECTION.

THE OUTPUT OF THE INPUT AMPLIFIER IS THEN MULTIPLIED BY SINωt AND COSωt REFERENCE SIGNALS, BY A TEMPERATURE STABILIZED MULTIPLIER. EACH OUTPUT IS INTEGRATED FOR A WHOLE NUMBER OF CYCLES OF THE TEST SIGNAL AS ESTABLISHED BY THE TIMING SYSTEM.

THE INTEGRATOR OUTPUTS ARE PUT INTO 'HOLD' FOR A SUFFICIENT TIME TO ALLOW THE COORDINATE COMPUTER TO SOLVE FOR PHASE AND AMPLITUDE.

THE INTEGRATORS ARE THEN 'RESET' FOR A MINIMUM TIME (SUFFICIENT TO INSURE A COMPLETE RESET TO ZERO), AND A NEW CYCLE OF ANALYSIS IS STARTED AT THE NEXT 1/4 CYCLE OF THE TEST FREQUENCY. THE RESET TIME AND START TIME ARE DETERMINED BY THE TIMER.

THE ANALYSIS OF THE RETURN SIGNAL IS AN EXACT MECHANIZATION OF THE FOURIER INTEGRAL. THIS GIVES VERY HIGH NOISE AND HARMONIC REJECTION IN THE SHORTEST TIME. THE RESULTS DEFINE THE FREQUENCY RESPONSE IN EXACT EQUIVALENCE TO 'DESCRIBING FUNCTION' THEORY. THE RESULTS ARE IDEAL FOR USE IN DETERMINING A MATHEMATICAL MODEL OF THE TRANSFER FUNCTION OF THE ITEM-UNDER-TEST.

THE END OF EACH CYCLE-OF-ANALYSIS IS INDICATED BY AN END-OF-CYCLE LIGHT. THE VARIATION OF THE READINGS AT ONE-FREQUENCY WITH TIME BECOMES A DIRECT MEASURE OF THE EFFECT OF NOISE ON THE RESULTS.

THE COORDINATE CONVERSION COMPUTER SOLVES THE CARTESIAN TO POLAR CONVERSION PROBLEM FROM THE IN-PHASE AND QUADRATURE COMPONENT INPUTS FROM THE INTEGRATORS. TWO CHANNELS ARE HANDLED SIMULTANEOUSLY, WITH AMPLITUDE CH#1, PHASE SHIFT, AMPLITUDE CH#2, AND AMPLITUDE RATIO RESULTING.

THE RESULTS ARE DISPLAYED ON TWO 3 1/2 DIGIT, BIPOLAR DIGITAL METERS; AND THEY ARE AVAILABLE AS D.C. VOLTAGES FOR PLOTTING. LOG FREQUENCY IS ALSO AVAILABLE TO DRIVE THE 'X' AXIS OF THE PLOTTER.

THE ENTIRE SYSTEM IS INTEGRATED TO MINIMIZE ANALYSIS TIME AND YET OBTAIN ACCURATE RESULTS UNDER VERY POOR SIGNAL TO NOISE RATIOS. THIS IS ACCOMPLISHED BY TWO MAJOR SYSTEMS - THE AUTOMATIC GAIN CONTROL AND THE TIMING SYSTEMS.

THE DUAL AUTOMATIC GAIN CONTROL SYSTEM ESTABLISHES THE OPTIMUM SENSITIVITY FOR EACH CHANNEL OF ANALYSIS. IT DISTINGUISHES BETWEEN SIGNAL UNDERLOAD, SIGNAL OVERLOAD, AND SIGNAL PLUS NOISE OVERLOAD. PRIORITY IS GIVEN TO CORRECTING NOISE OVERLOADS; GOING SO FAR AS TO PERMIT CONTINUED OPERATION AT SIGNAL UNDERLOAD WHEN THE NEXT HIGHER GAIN WOULD CAUSE A NOISE OVERLOAD. AT ALL TIMES, THE AUTOMATIC GAIN CONTROL SETS THE SENSITIVITIES AS WOULD AN 'ATTENTIVE' OPERATOR. IT ABSOLUTELY INSURES THAT THE OUTPUT IS THE RESULT OF A COMPLETE CYCLE OF ANALYSIS WITHOUT NOISE OVERLOAD, AND AT AS NEAR AN OPTIMUM GAIN AS THE NOISE LEVEL PERMITS. THE OPERATOR IS KEPT AWARE OF HOW THE AUTOMATIC GAIN CONTROL IS FUNCTIONING BY FRONT PANEL OVERLOAD AND UNDERLOAD LIGHTS.

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THE TIMING SYSTEM ESTABLISHES THE SEQUENCE OF INTEGRATE, HOLD AND RESET MODES. MOST IMPORTANTLY, IT MAKES THE INTEGRATE TIME EQUAL TO A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY (IN ALL BUT THE TWO HIGHEST FREQUENCY RANGES, WHERE A FIXED TIME IS USED). TWO INTEGRATE TIMES ARE AVAILABLE AT ALL OPERATING FREQUENCIES WITH THE LONGER ONE USED FOR GREATER NOISE REJECTION.

THE TIMING SYSTEM INTERLOCKS WITH THE AUTOMATIC GAIN CONTROL AND SWEEP SYSTEMS TO ABORT ANY CYCLES OF ANALYSIS WHICH ARE INVALIDATED BY NOISE OVERLOAD, FREQUENCY RANGE SWITCHING, END-OF-SWEEP, OR AN 'OFF' COMMAND. THUS, A SMOOTH, CONSISTANT PLOT RESULTS.

BUILT INTO EACH SUBSYSTEM OF THE MODEL 916 ARE CONTROLS WHICH IMPROVE THE APPLICATION OF THE FREQUENCY RESPONSE ANALYZER TO THE REAL PROBLEMS MET IN PERFORMING FREQUENCY RESPONSE MEASUREMENTS. THIS INCLUDES:

A FAST D.C. REJECT SWITCH TO SPEED UP REJECTION OF A D.C. OFFSET ON A RETURN SIGNAL.

AN ON-OFF SWITCH TO STOP THE ANALYZER AND RESET THE TEST SIGNAL ON COMMAND.

ADDED FILTERING TO ASSIST IN HIGH FREQUENCY NOISE REJECTION.

CONTINUOUS SWEEPS WITH OPERATOR CONTROL AT ALL TIMES OF SWEEP SPEED, AND AN ABILITY TO CHANGE SWEEP SENSE (FOR RETRACE OF A PORTION OF THE SWEEP), WITHOUT STOPPING THE TEST.

CONTINUOUS ADJUSTMENT OF TEST SIGNAL AMPLITUDE AND OFFSET, WITH METER READING OF OFFSET. SIN, TRIANGLE AND SQUARE WAVE TEST SIGNALS.

OPTIONS FOR CARRIER, REMOTE PROGRAMMING, TAPE, AMPLITUDE SERVO, ETC.

THE DUAL DIGITAL READOUT GIVES PRECISE DIRECT READING FREQUENCY, PHASE SHIFT, AMPLITUDE RATIO (DB), AMPLITUDE CH#1 (DB), AMPLITUDE CH#2 (DB), AND OFFSET. A CONNECTOR ON THE BACK PROVIDES REMOTE DIGITAL READOUT OF EITHER METER AS SWITCH OR ELECTRONICALLY SELECTED.

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916XH

FINALLY, ALL OF THE MEANS ARE INCLUDED TO DIRECTLY PLOT THE RESULTS OF AMPLITUDE RATIO (DB) AND PHASE SHIFT VS. LOG FREQUENCY. THE PROCEDURE IS COMPLETELY AUTOMATIC. THE OPERATOR NEED ONLY SET THE 'START' AND 'STOP' FREQUENCIES, AND THE SWEEP SPEED (VARIABLE IF DESIRED DURING THE TEST). CALIBRATE LEVELS ARE PROVIDED FOR THE PLOTTER. AT THE END-OF-THE-SWEEP, THE TEST SIGNAL IS TURNED OFF.

THE SWEEP SYSTEM IS CAREFULLY INTERLOCKED WITH AUTOMATIC GAIN CONTROL AND TIMING TO PREVENT ANY PORTION OF THE FREQUENCY RANGE FROM BEING BYPASSED.

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4.4 - TEST AND REFERENCE SIGNAL GENERATOR SYSTEM

REFERENCE: FIGS. 4.4-1, 4.4-2, AND 4.4-3

4.4.1 - FUNCTIONS

THE TEST AND REFERENCE SIGNAL GENERATOR PERFORMS ALL OF THE FOLLOWING FUNCTIONS:

1) SETS THE FREQUENCY OF THE ANALYZER IN RESPONSE TO FRONT PANEL START SWITCH AND POT (S1* & R1*).

2) GENERATES 10 VOLT PEAK SINE WAVE, COSINE WAVE, TRIANGLE WAVE AND SQUARE WAVE.

3) SWEEPS FREQUENCY IN ONE CONTINUOUS LOG SWEEP FROM ANY 'START' TO ANY 'STOP' FREQUENCY IN THE 6 1/2 DECADE FREQUENCY RANGE. SWEEP SPEED IS DETERMINED BY THE FRONT PANEL SWEEP SPEED SWITCHES (S3* & S4*).

   STOP FREQUENCY IS SET ON THE FRONT PANEL SWITCH AND POT (S2*, R2*).

   SWEEP MODE IS CONTROLLED BY S9* AS 'RESET', SWEEP (UP IN FREQUENCY), 'HOLD' WITH S14* GIVING A SWEEP DOWN CAPABILITY OVER A LIMITED FREQUENCY RANGE.

4) GENERATES A D.C. SIGNAL PROPORTIONAL TO LOG FREQUENCY TO DRIVE THE 'X' AXIS OF THE PLOTTER.

5) PROVIDES DRIVE TO ITEM-UNDER-TEST WITH SELECTABLE WAVESHAPE (S6*), D.C. OFFSET (R4*, S8*), PRECISE AMPLITUDE ADJUST R3*, S7*), AT ±30 MA, TO ±10 VOLTS.

* MOUNTED ON FRONT PANEL. LOCATED ON FRONT PANEL OF MODEL 916.

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4.4 - TEST AND REFERENCE SIGNAL GENERATOR SYSTEM

4.4.2 - FREQUENCY OF OPERATION - DCS1

REFERENCE: FIG. 4.4-1

THE D.C. VOLTAGE DEVELOPED BY A2 OF BOARD #2 COMMANDS FREQUENCY OF OPERATION. IT IS REFERRED TO AS 'DCS1' AND AS 'LIN FREQUENCY'.

THE THREE LINES OUR TO THE COUNTER UL1 ON BOARD #2 COMMAND FREQUENCY RANGE. THE CODING IS AS FOLLOWS:

FREQUENCY RANGE FULL SCALE		#	PIN '6' (5 + 6)	PIN 'L' (3 + 4)	PIN '10' (ALT)
1.0	HZ	1	0	0	0
10.0	HZ	2	0	0	1
100.	HZ	3	0	1	0
1	KHZ	4	0	1	1
10	KHZ	5	1	0	0
100	KHZ	6	1	0	1

THE D.C./FREQUENCY BOARD #10 CONVERTS THE THREE LINE LOGIC TO THE COMMANDED FREQUENCY RANGE AND CONVERTS THE DCS1 COMMAND TO THE FREQUENCY WITHIN THE FREQUENCY RANGE.

DCS1 IS SCALED, +10.0 VOLTS = FULL SCALE FREQUENCY. WITHIN THE FREQUENCY RANGE, FREQUENCY IS LINEARLY PROPORTIONAL TO DCS1.

WHEN THE ANALYZER IS IN 'RESET', FREQUENCY IS SET BY THE FRONT PANEL R1 POTENTIOMETER, AND FREQUENCY RANGE IS SET BY S1.

DURING SWEEP, DCS1 IS CHANGED BY THE SWEEP VOLTAGE, AND FREQUENCY RANGE IS CHANGED BY THE COUNTER ADVANCING. SEE SECTION 4.4.5 FOR SWEEP.

FREQUENCY RANGE SELECTS THE FEEDBACK CONDENSER AND THE INPUT RESISTOR OF THE INTEGRATOR IN THE D.C./FREQUENCY CONVERTER.

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4.4 - TEST AND REFERENCE SIGNAL GENERATOR SYSTEM

4.4.3 - SIN AND COSINE GENERATOR

REFERENCE: DRAWING C104473 SH. 1 OF 2

TWO DIODE FUNDCTION GENERATORS ON BOARD #9 ARE USED TO SHAPE THE SIN & COS TRIANGELS TO FORM '10 SIN ωt' AND '10 COS ωt'. POTS ARE PROVIDED TO PRECISELY SET AMPLITUDE AND ZERO D.C. LEVEL.

4.4.4 - TEST SIGNAL

REFERENCE: FIG. 4.4-1

THE SWITCHING TO SELECT WAVESHAPE AND AMPLITUDE RANGE, THE POT TO SET AMPLITUDE AND THE POWER AMPLIFIER, ARE ON THE FRONT PANEL.

THESE ARE DESIGNED FOR LOW NOISE, LOW DISTORTION, AND HIGH CURRENT CAPABILITY.

4.4.5 - FREQUENCY SWEEP SYSTEM

REFERENCE: BLOCK DIAGRAM OF FIG. 4.4-3

4.4.5.1 - SWEEP WITHIN ONE FREQUENCY RANGE

THE SWEEP IS CONTROLLED BY THE INTEGRATOR A1. WHEN THE SWEEP MODE SWITCH 'S9' IS IN RESET, A1 OUTPUT IS ZERO VOLTS. FREQUENCY IS SET BY THE START FREQUENCY POT 'A1' AS THE ONLY INPUT TO AMPLIFIER A2. 'A2' OUTPUT DIRECTLY COMMANDS THE D.C. TO FREQUENCY CONVERTER. 'A2' OUTPUT IS REFERRED TO AS DCS1.

WHEN THE SWEEP MODE SWITCH 'S9' IS SWITCHED TO 'SWEEP', 'A1' IS RELEASED TO INTEGRATE ITS INPUT CURRENT. THE INPUT IS DETERMINED BY THE SETTINGS OF 'S3', THE 10^N SEC./DECADE SWITCH AND BY 'S4', THE MULTIPLIER SWITCH. 'S3' SETS N = 1, 2, 3, 4. THE MULTIPLIER SETS X1, X.8, X.6, X.4, X.2 BY SETTING THE INPUT VOLTAGE TO 3, 3.75, 5.0, 7.5, 15 VOLTS, RESPECTIVELY. NOTE THAT SWEEP SPEED CAN BE CHANGED WITHOUT INTERRUPTING OR SHIFTING THE INTEGRATOR OUTPUT. ONLY THE SLOPE OF VOLTS VS. TIME CHANGES.

THE DIODE FUNCTION GENERATOR SHAPES THE LINEAR VOLTS VS. TIME TO A CURRENT INTO 'A2' WHICH VARIES LOGARITHMICALLY WITH TIME. THUS, AT ONE SWEEP SPEED, THE TIME SPENT GOING FROM ONE HZ TO TWO HZ, IS THE SAME AS FROM 2 TO 4, 4 TO 8, OR 5 TO 10. THIS WEIGHTING IS SELECTED TO MATCH THE GEOMETRIC PROPERTY OF CIRCUITS AND SYSTEMS VS. FREQUENCY.

SWEEP IS STOPPED BY THE COMPARATOR (A3) RECOGNIZING THAT THE STOP FREQUENCY (R2 SETTING) HAS BEEN REACHED.

4.4.5.2 - FREQUENCY RANGE SWITCHING

THE 'START FREQUENCY RANGE' IS SET INTO THE ANALYZER BY 'S1'. ITS THREE BIT BINARY CODED OUTPUT 'PRESETS' THE COUNT OUTPUT OF 'UL1' WHEN THE SWEEP MODE SWITCH 'S9' IS IN RESET. THE COUNT OUTPUT OF 'UL1' COMMANDS THE FREQUENCY RANGE OF THE 916 (DC/FREQUENCY CONVERTER, TIMING SYSTEM, ETC.).

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AS LONG AS 'S9' IS LEFT IN 'RESET', THE COMMANDED FREQUENCY RANGE IS THE OPERATING FREQUENCY RANGE. THE LEFT HAND CABLE BOARD HAS A DIGITAL COMPARATOR 'UL1' WHICH COMPARES THE COMMANDED FREQUENCY RANGE FROM COUNTER 'UL1' WITH START FREQUENCY RANGE FROM 'S1'. ITS LOGIC LEVEL OUTPUT DRIVES THE START FREQUENCY RANGE SELECTOR. AS LONG AS THE OPERATING FREQUENCY RANGE IS THE SAME AS THE START FREQUENCY RANGE, THE START FREQUENCY OUTPUT OF 'R1' IS AN INPUT TO 'A2'. THIS SETS THE START FREQUENCY FOR THE SWEEP.

A SECOND DIGITAL COMPARATOR (UL2 ON LEFT HAND CABLE BOARD), COMPARES THE STOP FREQUENCY RANGE SETTING OF S2 WITH THE OPERATING FREQUENCY RANGE FROM THE COUNTER 'UL1'. THE 'STOP FREQUENCY RANGE SELECTOR' IS OPERATED BY THE 'UL2' COMPARATOR OUTPUT.

IF THE OPERATING FREQUENCY RANGE IS THE SAME AS THE STOP FREQUENCY RANGE, THE STOP FREQUENCY VOLTAGE FROM R2 IS MADE THE INPUT TO THE A3 COMPARATOR, AND IT DETERMINES THE DCS1 VALUE (OR FREQUENCY) AT WHICH THE SWEEP STOPS. THE STOP FREQUENCY RANGE COMPARATOR ALSO DISABLES THE UL3 ONE-SHOT.

IF, HOWEVER, THE STOP FREQUENCY RANGE IS HIGHER THAN THE START FREQUENCY RANGE, THE UL2 COMPARATOR CAUSES THE SELECTOR TO USE THE '100% OF RANGE INPUT' AS THE REFERENCE TO THE A3 COMPARATOR. THUS, THE SWEEP GOES TO FULL SCALE (REGARDLESS OF R2 SETTING) AND A3 TRIPS.

FREQUENCY RANGE IS STEPPED UP ONE BY A3 TRIGGERING THE ONE-SHOT UL3, WHICH, IN TURN, ADVANCES THE COUNTER (RELEASED FROM PRESET WHEN S9 WAS PUT IN SWEEP) BY ONE COUNT. AT THE SAME TIME: THE INTEGRATOR IS RESET TO ZERO; AND THE START FREQUENCY RANGE COMPARATOR 'UL1' INDICATES THAT THE OPERATING FREQUENCY RANGE IS NOT EQUAL TO THE START FREQUENCY RANGE (S1 SETTING). THIS, IN TURN, MOVES THE 'START FREQUENCY SELECTOR' TO COMMAND 10.0% OF FULL SCALE AS THE INPUT TO A2. THE NET RESULT IS THAT THE FREQUENCY REMAINS NEARLY CONSTANT GOING FROM 100% OF ONE FREQUENCY RANGE TO 10% OF THE FOLLOWING FREQUENCY RANGE.

NOT SHOWN ON THE DIAGRAM ARE THE MEANS TAKEN TO INSURE THAT THE SWITCHING IS SMOOTH, AND TO ABORT THE CYCLE-OF-ANALYSIS WHICH OCCURS DURING THE FREQUENCY RANGE SWITCHING OPERATION.

THE SWEEP IS RELEASED AND THE NEW FREQUENCY RANGE IS SWEPT THROUGH FROM 10% TO 100% OF FULL SCALE. THIS CONTINUES UNTIL THE FREQUENCY RANGE IS REACHED WHICH CORRESPONDS TO THE STOP FREQUENCY RANGE SET BY S2. THEN, THE LOGIC OUT OF THE STOP FREQUENCY RANGE COMPARATOR UL2 COMMANDS THE STOP FREQUENCY RANGE SELECTOR TO USE THE OUTPUT OF THE STOP FREQUENCY POT R2 AS THE COMPARATOR INPUT. IN STOP FREQUENCY RANGE, THE ONE-SHOT, WHICH ADVANCES THE FREQUENCY RANGE COUNTER, IS INHIBITED. FREQUENCY RANGE CANNOT ADVANCE TO A HIGHER FREQUENCY RANGE.

THE 'END-OF-SWEEP' LOGIC DETERMINES THAT THE FOLLOWING COMBINATION OF EVENTS HAVE OCCURRED:

FREQUENCY RANGE IS THE STOP FREQUENCY RANGE; AND THE SWEEP IS NOT IN 'RESET'

THEN, WHEN THE COMPARATOR A3 FLIPS (FREQUENCY HAS REACHED STOP FREQUENCY), A LOGIC LEVEL IS GENERATED WHICH TURNS OFF THE TEST SIGNAL, ABORTS THE ANALYSIS CYCLE, RETURNS THE TIMING TO 'RESET', AND SIGNALS 'STOP' ON THE FRONT PANEL LIGHT DS9.

NOT SHOWN IS THE COMMAND TO THE SWEEP INTEGRATOR TO GO INTO 'HOLD'.

NOTE THAT THE FREQUENCY DISPLAY FOLLOWED THE FREQUENCY AS IT SWEPT FROM THE START TO THE STOP VALUE.

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4.5 - RETURN SIGNAL FOURIER ANALYZERS - INCLUDING INPUT PREAMPLIFIER & AMPLIFIER

REFERENCE: FIG. 4.5-1

4.5.1 - INPUT PREAMPLIFIER & INPUT AMPLIFIER

4.5.1.1 - THE MATCHED FILTER COMMON TO BOTH CHANNELS OF THE 916

THERE ARE SEVERAL FILTERS IN EACH CHANNEL OF ANALYSIS. IN EACH CASE, THE FILTER TIME CONSTANTS ARE MATCHED SO THAT THEY PRODUCE THE SAME PHASE SHIFT AND ATTENUATION VS. FREQUENCY IN EACH CHANNEL. THE FILTERS IMPROVE THE NOISE REJECTION CAPABILITIES OF THE 916.

SINCE THE PHASE SHIFT COMPUTATION IS OF $[\angle CH\#2 - \angle CH\#1]$, THEIR NET EFFECT ON THE RESULT IS NEGLIGIBLE. ALSO, AS THE AMPLITUDE RATIO IS 'AMP DB CH#2 - AMP DB CH#1', THEIR NET EFFECT ON AMPLITUDE RATIO IS NEGLIGIBLE.

THIS IS ALSO THE BASIS FOR OPERATING THE MODEL 916 WITH EXTERNAL FILTERS (DUAL MATCHED) FOR EXTREME CASES OF POOR SIGNAL TO NOISE RATIOS (SEE SEC. 3.4.6 & 3.8).

EACH FILTER DOES HAVE AN EFFECT ON THE AMP CH#1 (DB) AND THE AMP CH#2 (DB). WHERE THIS EFFECT IS LARGER THAN 0.1 DB, CURVES ARE PROVIDED TO CORRECT THESE RESULTS FOR THE ATTENUATION OF THE FILTER.

THIS AGAIN IS ONE AREA WHERE THE TWO CHANNEL ANALYZER IS SUPERIOR TO THE SINGLE CHANNEL ONE. FILTERS CAN BE USED WITH THE TWO CHANNEL ANALYZERS WITHOUT EFFECTING THE AMP RATIO (DB) AND PHASE SHIFT RESULTS AS LONG AS THE FILTERS ARE MATCHED IN THE TWO CHANNELS.

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4,5.1.2 - RETURN SIGNAL INPUT CIRCUIT

REFERENCE: FIG. 4.5-1

A) A.C. COUPLED

THE RETURN SIGNAL IS A.C. COUPLED (R_1C_1) TO A HIGH INPUT IMPEDANCE FOLLOWER AMPLIFIER. THE TRANSFER FUNCTION IS-

$$\frac{R_1C_1j\omega}{1 + R_1C_1j\omega} \qquad (4.5\text{-}1)$$

THE BREAK FREQUENCY IS:

$$F_1 = \frac{1}{2\pi R_1C_1} \qquad (4.5\text{-}2)$$

FOR THE 916, F_1 = .008 HZ (4.5-3)

AND - FOR THE 916H, F_1 = .040 HZ (4.5-4)

FOR THE 916XH, F_1 = .040 HZ (4.5-4)

BOTH CHANNELS OF THE ANALYZER ARE MATCHED SO THAT THERE IS NO EFFECT ON AMP RATIO (DB) AND PHASE SHIFT. FIG. 4.5-2A IS PROVIDED TO SHOW THE EFFECT ON AMP CH#1 (DB) OR AMP CH#2 (DB) RESULTS IN THE LOWEST FREQUENCY RANGE OF THE HIGH PASS INPUT FILTER.

THE HIGH PASS FILTER REJECTS D.C. OFFSET ON THE RETURN SIGNAL TO ±100 VOLTS. IT ALSO ATTENUATES SLOW VARIATIONS IN THE RETURN SIGNAL WITH FREQUENCY COMPONENTS BELOW F_1.

TO PREVENT MORE THAN ±20 VOLTS TO OCCUR AT THE CIRCUIT INPUT, (AND THUS PREVENT DAMAGE TO THE I.C.S.), DUAL 20 VOLT ZENERS LIMIT THE CONDENSER OUTPUT TO ±20 VOLTS. THEY ALSO PROVIDE A LOW RESISTANCE PATH TO GROUND WHEN MORE THAN 20 VOLTS D.C. IS APPLIED BY THE RETURN SIGNAL TO CHARGE THE CONDENSER RAPIDLY TO (INPUT -20) VOLTS D.C.

TO SPEED UP THE CHARGING OF THE INPUT CONDENSER, THE OPERATOR DEPRESSES 'FAST D.C. REJECT' SWITCH (S11 OR S12). THIS IS A MOMENTARY SWITCH WHICH CONNECTS THE CONDENSER OUTPUT TO GROUND THRU A LOW VALUE RESISTOR. 'FAST D.C. REJECT' IS USED WHEN THE D.C. LEVEL OF THE RETURN SIGNAL IS FIRST APPLIED OR A LARGE CHANGE IS MADE IN THE OPERATING POINT.

A.C. COUPLING OF THE RETURN SIGNAL IS ONE OF THE IMPORTANT CHARACTERISTICS OF THE MODEL 916. IT SPEEDS UP THE TEST PROCESS, IT SIMPLIFIES THE ELECTRONICS, AND IT REJECTS LOW FREQUENCY NOISE.

B) BALANCED INPUT -

A FULLY BALANCED INPUT PREAMPLIFIER IS INCLUDED SO THAT BOTH ENDS OF THE RETURN SIGNAL CAN BE OFF OF GROUND. A REASONABLE LEVEL OF COMMON MODE REJECTION IS BUILT IN TO ASSIST IN REJECTING NOISE COMMON TO BOTH SIGNAL LEADS.

C) INPUT FILTER - FILTER 'IN-OUT' - S13 -

THE OPERATOR HAS THE OPTION OF TURNING ON AN ADDITIONAL LOW PASS FILTER WHICH HAS A TRANSFER FUNCTION OF -

$$\frac{1}{T_2 J\omega + 1} \qquad (T_2 = R_f C_f) \qquad (4.5\text{-}5)$$

THIS ASSISTS IN REJECTING HIGH FREQUENCY NOISE TERMS. C_f IS NORMALLY SELECTED TO BREAK AT 12 KHZ. (OTHER BREAK POINTS ARE AVAILABLE AS REQUESTED). ITS EFFECT ON THE AMP CH#1 (DB) AND AMP CH#2 (DB) IS SHOWN IN FIG. 4.5-2B. AGAIN, IT IS MATCHED IN BOTH CHANNELS TO HAVE NO EFFECT ON AMP RATIO (DB) AND PHASE SHIFT.

D) INPUT FOLLOWER -

THE INPUT TO THE FOLLOWER AMPLIFIER (AT 4 MEGOHMS IN THE 916 - TWO - 2 MEGOHM RESISTORS; AND AT 800 K IN THE 916H & XH - TWO 400 K RESISTORS) HAS A SMALL TRIM CONDENSER TO MATCH THE HIGH FREQUENCY PHASE RESPONSE, CANCEL OUT THE VARIATION IN INPUT CAPACITANCE OF THE FOLLOWER AMPLIFIER AND TO PREVENT AMPLIFIER MALFUNCTION DUE TO EXCESSIVE VERY HIGH FREQUENCY NOISE.

FIGURE 4.5-2C PLOTS THE CORRECTION CURVE TO AMP CH#1, AMP CH#2 FOR OPERATION OF THE MODEL 916 FROM 2 KHZ TO 10 KHZ. THE BAND SHOWN IS THE VARIATION FROM UNIT TO UNIT OF 916 PRODUCTION. A MEASUREMENT ON THE 916 WITH OUTPUT RETURNED TO THE INPUT ESTABLISHES TO ± .1 DB, THE APPLICABLE CORRECTION CURVE.

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4.5.1.3 - INPUT AMPLIFIER

THE INPUT AMPLIFIER ALSO HAS A HIGH PASS FILTER ACTION. ITS TRANSFER FUNCTION IS:

$$\frac{\text{OUTPUT}}{\text{INPUT}} = \frac{\left(\frac{50}{\text{F.R.}} - j\mathcal{f}\right) \quad \text{(GAIN)}}{1 + \frac{50}{\text{F.R.}} j\mathcal{f}} \qquad (4.5\text{-}6)$$

F.R. = FREQUENCY RANGE (FULL SCALE)
$\mathcal{f}$ = FREQUENCY OF OPERATION (HZ)

THE BREAK FREQUENCY IS APPROXIMATELY 1/250 OF FULL SCALE FREQUENCY RANGE. FOR EXAMPLE, WHEN IN THE 50 HZ RANGE, F_2 = .2 HZ; ETC.

AS FREQUENCY RANGE CHANGES, (MANUALLY OR IN SWEEP), THE FILTER BREAK FREQUENCY MOVES TO THE VALUE FOR THE FREQUENCY RANGE IN USE.

THIS HIGH PASS FILTER ENHANCES THE HIGH PASS ACTION OF THE INPUT HIGH PASS FILTER. IT BECOMES FASTER AS THE FREQUENCY INCREASES, WHICH GREATLY IMPROVES THE REJECTION OF NOISE AT FREQUENCIES BELOW THE TEST FREQUENCY. THE REDUCTION OF D.C. OUTPUT OF THE INPUT AMPLIFIER TO ZERO BY THIS FILTER PERMITS THE FULL USAGE OF THE MULTIPLIERS'S DYNAMIC RANGE IN REJECTING HIGHER FREQUENCY NOISE TERMS.

THE INPUT AMPLIFIER COMBINES A GAIN RANGE AS COMMANDED BY THE AUTOMATIC GAIN CONTROL SYSTEM FROM 1 VOLT/VOLTS, TO 1024 VOLTS/VOLT IN 'X2' INCREMENTS.

THUS, THE INPUT AMPLIFIER FILTER REMAINS UNCHANGED IN THE 916XH. IT IS NOW DOWN 250/1 FROM FULL SCALE. THE EFFECT ON AMP CH#1, #2 IS NEGLIGIBLE.

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4.5.2 - FOURIER INTEGRAL MECHANIZATION

THE MULTIPLIER - INTEGRATOR BOARDS PERFORM THE FOURIER INTEGRAL MECHANIZATION. THE RETURN SIGNAL IS MULTIPLIED BY THE SIN AND COS REFERENCE SIGNALS, THE PRODUCTS ARE ATTENUATED PROPORTIONAL TO (DCS1/10), AND THE RESULTS ARE INTEGRATED.

THE TRANSCONDUCTANCE MULTIPLIER WAS SELECTED BECAUSE OF ITS WIDE BANDWIDTH AND BECAUSE OF ITS LINEARITY IN THE FUNCTION REQUIRED. TO IMPROVE ITS PERFORMANCE, THE ZERO ADJUST IS HIGHLY STABILIZED.

THE ATTENUATOR CIRCUIT IS DISCUSSED IN SECTION 4.9.1.

THE INTEGRATOR AMPLIFIER IS A VERY STABLE FET INPUT I.C. IT IS INSTALLED WITH HOLD, OPERATE AND RESET MODES. THE INTEGRATOR IS GIVEN A COMMON SPAN BY THE SELECTION OF CAPACITOR VALUES WITHIN LESS THAN '1/2%' OF VALUE.

WHENEVER THE INTEGRATOR IS IN 'RESET', IT IS ALSO IN 'HOLD' (SEE SEC. 5.16 - TIMING BOARD). THIS KEEPS THE MULTIPLIER OUTPUT FROM EFFECTING THE RESET TO ZERO (IN RESET THERE IS A FINITE FEEDBACK 'R').

THE INTEGRATORS IN 'RESET' HAVE ZERO OUTPUT. IN 'OPERATE' EACH INTEGRATOR, INTEGRATES THE INPUT FROM THE MULTIPLIER-ATTENUATOR. IN 'HOLD', THE INTEGRATOR OUTPUT STAYS CONSTANT AT ITS LAST VALUE. THEN THE INTEGRATOR IS RESET TO ZERO, AND ANOTHER CYCLE OF ANALYSIS BEGINS. (DURING 'HOLD', THE PHASE, AMPLITUDE, ETC., ARE DETERMINED AND ARE READ INTO THE OUTPUT).

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4.6 - TIMING SYSTEM - REFERENCE: FIG. 4.6-1

4.6.1 - OVERALL

THE TIMING SYSTEM IS SHOWN AS A BLOCK DIAGRAM IN FIG. 4.6.1. THERE IS ALSO A TIMING DIAGRAM.

THE TIMING SYSTEM LOCKS THE OPERATING TIME OF THE INTEGRATORS TO THE FREQUENCY OF OPERATION AND TO THE STATUS OF THE 'X5' COMMAND.

THE TIMING SYSTEM SEQUENCES THE THREE MODES OF THE INTEGRATORS (RESET, OPERATE, HOLD) AND LOCKS THE READ-HOLD MODES OF THE PHASE, AMP (DB), AMPLITUDE RATIO (DB) READOUTS TO THE INTEGRATOR SEQUENCE.

FINALLY, THE TIMING SYSTEM INTERLOCKS APPROPRIATELY WITH THE AUTOMATIC GAIN CONTROL SYSTEM, THE ON-OFF SWITCH, FREQUENCY RANGE SWITCHING (IN SWEEP) AND END OF SWEEP.

ALL OF THE ABOVE ARE DONE IN CONTINUOUS SYNCHRONIZATION WITH THE OPERATING FREQUENCY SO THAT THEY ARE FUNCTIONING CORRECTLY IN SWEEP MODE.

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4.6.2 - INTEGRATE TIME

AS SHOWN IN SECTION 4.2, HARMONIC REJECTION IS DIRECTLY RELATED TO INTEGRATION BEING TIMED FOR A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY. IN THE FOUR LOW FREQUENCY RANGES, THE INTEGRATE TIME IS PRECISELY RELATED TO THE NUMBER OF CYCLES OF THE TEST FREQUENCY AS:

FREQUENCY	#CYCLES OF TEST FREQUENCY			
	X5	(# OF PULSES)	X5	(# OF PULSES)
.025 HZ - .50 HZ	1	(4)	2	(8)
.25 HZ - 5.0 HZ	1	(4)	2	(8)
2.5 HZ - 50.0 HZ	2	(8)	10	(40)
25.0 HZ - 500 HZ	20	(80)	100	(400)

THIS IS ACCOMPLISHED BY:

1) GENERATING FOUR PULSES PER CYCLE AT PRECISE TIMES ON THE CYCLE.

2) COUNTING THESE PULSES UNTIL THE NUMBER IS REACHED CORRESPONDING TO THE ABOVE NUMBER OF CYCLES OF THE TEST FREQUENCY.

3) TAKING THE INTEGRATORS OUT OF 'RESET' AT THE START OF THIS COUNT AND PUTTING THE INTEGRATORS INTO 'HOLD' AT THE END OF THE COUNT.

IN THE TWO HIGH FREQUENCY RANGES, INTEGRATE TIME HAS A VALUE OF .036 SEC. FOR '$\overline{X5}$' (OUT), AND OF .18 SEC. FOR 'X5' (IN). THE NUMBER OF CYCLES INTEGRATED OVER IS LARGE ENOUGH SO THAT NEGLIGIBLE ERROR RESULTS FROM THE FIXED INTEGRATE TIME.

THE FIXED TIME IS COMPUTED FROM THE VERY STABLE 7 KHZ REFERENCE BY THE SAME SEQUENCE OF OPERATIONS AS GIVEN ABOVE.

4.6.3 - 'HOLD'

THE INTEGRATORS ARE PUT INTO 'HOLD' BY A 'ONE-SHOT' TRIGGERED BY THE END OF THE COUNT.

DURING 'HOLD' THE FOLLOWING OCCURS:

1) THE TIMING SEQUENCE IS LOCKED INTO 'HOLD' SO THAT NO OTHER EVENT IN THE ANALYZER CAN FORCE IT INTO 'RESET' UNTIL THE FULL 'HOLD' TIME IS OVER.

2) A FIXED TIME AFTER 'HOLD' STARTS, THE READOUT CIRCUITS ARE COMMANDED TO 'READ' THE RESULTS OF THE LAST ANALYSIS CYCLE. THE TIME DELAY ALLOWS THE PHASE, AMPLITUDE, AND DB CIRCUITS TO SETTLE OUT.

3) AT THE END OF THE INTEGRATE HOLD TIME, THE READOUT CIRCUITS ARE RETURNED TO 'HOLD', AND THE TIMING IS SEQUENCED INTO RESET (HOLD ONE-SHOT TIME ENDS AND TRIGGERS 'RESET' ONE-SHOT).

4.6.4 - RESET

THE MINIMUM 'RESET' TIME IS ESTABLISHED BY THE 'RESET ONE-SHOT'. IT ALSO SETS A FLIP-FLOP TO COMMAND RESET OF THE ANALYZER (INTEGRATORS).

THE RESET ONE-SHOT ESTABLISHES THE MINIMUM RESET TIME. WHEN THE RESET ONE-SHOT TIMES OUT, THE RESET FLIP-FLOP IS RETURNED TO ITS 'OPERATE' STATE BY THE NEXT PULSE FROM THE '4 PULSE/CYCLE' GENERATOR CIRCUIT (THRU THE 'AND-2' GATE). THUS, AT VERY LOW TEST FREQUENCIES, THE RESET TIME WILL BE 1/4 CYCLE OF THE TEST FREQUENCY. AT HIGHER FREQUENCIES, RESET TIME = .2 SEC. PLUS AT MOST 1/4 CYCLE OF THE TEST FREQUENCY.

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4.6.5 - INTERLOCKS OF TIMING

1) WITH ON-OFF

WHEN THE ANALYZER IS TURNED 'OFF', THE TIMING IS TRIGGERED INTO 'RESET' UNLESS THE SWITCHING TIME CORRESPONDS WITH THE 'HOLD' MODE. THEN 'RESET' IS BROUGHT ABOUT BY THE END OF 'HOLD'. A PARTIALLY COMPLETED ANALYSIS CYCLE IS ABORTED.

THE 'OFF' COMMAND (OF S5), ALSO BLOCKS THE PULSES WHICH NORMALLY RELEASE THE 'RESET' FLIP-FLOP FROM 'RESET' TO OPERATE. TIMING REMAINS IN 'RESET' UNTIL S5 IS PUT 'ON' BY THE OPERATOR.

2) WITH NOISE OVERLOAD

THE OCCURRENCE OF A NOISE OVERLOAD, GENERATES A PULSE WHICH TRIGGERS THE 'RESET' ONE-SHOT. A PARTIALLY COMPLETED CYCLE OF ANALYSIS IS ABORTED. THE GAIN IS REDUCED BY 1/2 AND THE ANALYSIS CYCLE STARTS OVER.

IF THE TIMING IS IN 'HOLD' WHEN THE OVERLOAD OCCURS, THE OVERLOAD PULSE DOES NOT ALTER THE SEQUENCE OF THE TIMING CIRCUIT. THE RESULTS OF THE LAST ANALYSIS CYCLE ARE COMPUTED AND READ INTO THE OUTPUT WHILE THE GAIN IS REDUCED BY 1/2. THE INTEGRATE PORTION OF THE ANALYSIS CYCLE WAS COMPLETED BEFORE OVERLOAD OCCURRED. IT IS A VALID ANALYSIS AND THE RESULTS ARE READ OUT.

3) FREQUENCY RANGE SWITCHING

DURING SWEEP, FREQUENCY RANGE SWITCHING GENERATES A PULSE WHICH IS USED TO PUT TIMING INTO 'RESET'. THIS ABORTS THE CYCLE OF ANALYSIS SO THAT ANY SWITCHING TRANSIENTS ARE NOT A PART OF THE RESULTS.

AGAIN, IF THE TIMING SEQUENCE IS IN 'HOLD', FREQUENCY RANGE SWITCHING DOES NOT MODIFY THE TIMING SEQUENCE. THE HOLD AND RESET TIMES ARE LONG ENOUGH FOR THE SWITCHING TRANSIENT TO SETTLE OUT.

4) END-OF-SWEEP

THE END-OF-SWEEP SIGNAL BLOCKS THE START OF A NEW CYCLE OF ANALYSIS. (IT ALSO PUTS SWEEP INTO 'HOLD' AND RESETS THE TEST SIGNAL). IT ACTS AT 'AND-2' INPUT (OF FIG. 4.6-1) JUST AS THE 'ON-OFF' SWITCH.

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5) SUMMARY

THUS, THE TIMING SEQUENCE CAN BE INTERRUPTED BY A NOISE OVERLOAD, BY THE 'ON-OFF' SWITCH (IN OFF) AND BY FREQUENCY RANGE SWITCHING.

IF THE TIMING IS IN 'RESET', IT IS RETURNED TO THE START OF THE RESET TIME.

IF THE TIMING IS IN 'OPERATE' (INTEGRATE), THE ANALYSIS CYCLE IS ABORTED AND RETURNED TO 'RESET'.

IF THE TIMING IS IN 'HOLD', TIMING IS LEFT TO CONTINUE IN THE NORMAL FASHION. THE RESULTS OF THE COMPLETED CYCLE OF ANALYSIS ARE ENTERED INTO THE OUTPUT. THE MODE SWITCHES TO RESET.

THE 'OFF' COMMAND FROM THE FRONT PANEL S5, AND THE 'END-OF-SWEEP' SIGNAL BLOCK THE PULSES FROM STARTING A NEW CYCLE OF ANALYSIS. THE ANALYZER STAYS IN RESET.

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4.7 - OUTPUT COMPUTATION

4.7.1 - PHASE & AMPLITUDE

REFERENCE: FIG. 4.7-1

(1) INTRODUCTION

THE IN-PHASE AND QUADRATURE D.C. LEVELS AT THE INTEGRATOR OUTPUTS FOR CH#1 AND CH#2 DEFINE TWO VECTORS OF AMPLITUDE C1 AND AT AN ANGLE θ_1 TO THE REFERENCE; AND OF AMPLITUDE C2 AT AN ANGLE θ_2 TO THE REFERENCE. C1, C2 AND $(\theta_2-\theta_1)$ ARE FOUND BY CONVERTING THE INTEGRATOR OUTPUTS TO A.C. SIGNALS USING A 7 KHZ CARRIER FREQUENCY AND SOLVING THE COORDINATE CONVERSION ON AN A.C. BASIS.

(2) MODULATION

7 KHZ SQUARE WAVES ARE GENERATED AT 0°, AND 90° PHASE RELATIONSHIP (ON 7 KHZ BD.#15). THE IN-PHASE COMPONENTS OF CH#1 AND CH#2 ARE SQUARE WAVE MODULATED BY THE 0° REFERENCE. THE QUADRATURE COMPONENTS OF CH#1 AND CH#2 ARE SQUARE WAVE MODULATED BY THE 90° REFERENCE.

(3) SUM & FILTER

THE IN-PHASE AND QUADRATURE COMPONENTS OF EACH CHANNEL ARE SUMMED AND FILTERED. THE FILTER COMBINES A SINGLE TIME CONSTANT AND A 0.4 DAMPING FACTOR QUADRATIC HAVING A 7 KHZ RESONANT FREQUENCY.

THE INPUTS ARE SQUARE WAVES WITH THIRD HARMONIC CONTENT OF 1/3RD-3RD, 1/5TH-5TH, ETC. THE FILTER ATTENUATES THE THIRD HARMONIC SUFFICIENTLY TO REDUCE THIRD HARMONIC DISTORTION TO 1% RMS. THIS REDUCES THE HIGHER HARMONICS EVEN MORE, AND RESULTS IN A GOOD SINE WAVE AT THE FILTER OUTPUT.

THE FILTER OUTPUT MAY BE EXPRESSED AS -

$$C1 \sin(\omega\tau + \theta_F + \theta_1) \qquad (4.7\text{-}1)$$

WHERE:

$$C1 = K(I_1^2 + Q_1^2)^{1/2} \qquad (4.7\text{-}2)$$

θ_F = FILTER PHASE SHIFT AT 7 KHZ

θ_1 = ARC-TAN Q_1/I_1

K = CONSTANT OF MODULATOR, FILTER GAIN

AT THE FILTER OUTPUT, IT IS EVIDENT THAT THE COORDINATE CONVERSION NOW IS AN A.C. PROBLEM, WHOSE SOLUTION INVOLVES:

(A) SOLVING FOR THE AMPLITUDE OF EACH SINE WAVE AS THE AMPLITUDE OF C1, AND C2 RESPECTIVELY.

(B) COMPARING ZERO CROSSOVERS OF THE TWO SINE WAVES FOR PHASE SHIFT OF (CH#2-CH#1), NOTE THAT θ_F (FILTER PHASE SHIFT) CANCELS OUT AS IT IS THE SAME FOR BOTH CHANNELS).

(4) SQUARING OF FILTER OUTPUT

IN EACH CHANNEL, A HIGH ACCURRACY, HIGH STABILITY ZERO CROSSING DETECTOR IS USED TO GENERATE A SQUARE WAVE WHICH SWITCHES AT THE ZERO CROSSINGS OF THE 7 KHZ SINE WAVE FILTER OUTPUT.

(5) AMPLITUDE DETERMINATION - EACH CHANNEL

THE SQUARE WAVE DRIVES THE HALF-WAVE DEMODULATOR IN SYNCHRONISM WITH THE FILTER OUTPUT. THE MINUS PORTION OF THE SINE WAVE IS TRANSMITTED TO A FILTER AND A READ-HOLD CIRCUIT. THE SIGN INVERSION OF THE READ-HOLD CIRCUIT GIVES POSITIVE OUTPUT DIRECTLY PROPORTIONAL TO C1 (OR C2 IN CH#2).

(6) PHASE SHIFT

EACH SQUARE WAVE TRIGGERS A ONE-SHOT THAT GENERATES A NARROW PULSE AT ONE OF THE SQUARE WAVE TRANSITIONS.

ONE PULSE 'SETS' THE FLIP-FLOP. THE OTHER PULSE 'RESETS' THE FLIP-FLOP.

THE BUFFER OUTPUT IS A SQUARE WAVE WHOSE 'ON' TIME AND 'OFF' TIME ARE BEING ESTABLISHED BY THE RELATIVE TIMES OF THE PULSES WHICH, IN TURN, IS ESTABLISHED BY THE PHASE SHIFT BETWEEN THE TWO SINE WAVES.

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(6) PHASE SHIFT

TO BE EXACT,

$$\text{PHASE SHIFT} = 180^\circ \left[\frac{\text{'ON' TIME} - \text{'OFF' TIME}}{\text{TIME PER CYCLE}}\right]$$

NOTE: WHEN 'ON' TIME = 'OFF' TIME,

PHASE SHIFT = 0°

THIS IS CONVERTED TO A D.C. VOLTAGE BY THE FET SWITCH Q1 SWITCHING THE INPUT TO THE FILTER AMPLIFIER FROM GROUND TO +15 THRU R1, R2. A SECOND AMPLIFIER PROVIDES ADDITIONAL FILTERING AND READ-HOLD ACTION ON THE OUTPUT. A DIRECT READING ±1.80 VOLTS INDICATING ±180° RESULTS.

(7) TIMING

THE PHASE AND AMPLITUDE COMPUTER IS PROGRAMMED BY THE TIMING SYSTEM. THIS INCLUDES THE READ-HOLD COMMAND, AND (NOT SHOWN ON 4.7-1), AN INHIBIT COMMAND TO THE SQUARING CIRCUITS DURING ANALYZER RESET MODE TO PREVENT OSCILLATION WHILE 'I' AND 'Q' ARE ZERO, AND ONLY NOISE IS PRESENT AS AN INPUT.

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4.7.2 - AMPLITUDE (DB), AMP RATIO (DB)

REFERENCE: FIG. 4.7-2, & DRAWING NO. C103395

THE DETERMINATION OF AMPLITUDE CH#1, AS DESCRIBED IN SEC. 4.7.2, DOES NOT INCLUDE THE CHANNEL SENSITIVITY. TO REFLECT THE RESULTS BACK TO THE SIGNAL LEVEL AT THE MODEL 916 INPUT, IT IS NECESSARY TO INCLUDE THE GAIN SETTING OF THE RESPECTIVE INPUT AMPLIFIER. THIS IS ACCOMPLISHED ON A LOG (DB) BASIS.

EACH INPUT AMPLIFIER BOARD HAS A LOG GAIN TO D.C. CONVERTER. THE GAIN COMMANDS FROM THE AUTOMATIC GAIN CONTROL SYSTEM ON BD. #5, SWITCHES CURRENT INTO AMP 5 SUCH THAT AMP 5 OUTPUT IS THE GAIN IN DB SCALED .1 VOLT/DB, AS FOLLOWS:

OUTPUT VOLT	GAIN - VOLTS/VOLT	OUTPUT VOLT	GAIN - VOLTS/VOLT
+ 0	1.0	+3.0	32
+ .6	2.0	+3.6	64
+1.2	4.0	+4.2	128
+1.8	8.0	+4.8	256
+2.4	16.	+5.4	512
		+6.0	1024

ON BOARD #12, EACH AMPLITUDE SIGNAL FROM ITS PHASE AND AMPLITUDE COMPUTER IS CONVERTED TO LOG AMPLITUDE. THIS COVERS AT MOST A 10/1 RANGE OF INPUT, AND IS USUALLY LIMITED TO A 4/1 RANGE.

THEN, THE FINAL STEP OF COMBINING LOG GAIN WITH LOG AMPLITUDE IN A3 FOR CH#1, AND A4 FOR CH#2 WITH THE CORRECT SENSE AND SCALE FACTOR TO PRODUCE AN OUTPUT WHICH IS THE AMPLITUDE OF THE RETURN SIGNAL IN DB. THE ZERO IS SET FOR DB = 1.0 VOLT PEAK OF SIGNAL CONTENT.

THE READ-HOLD ACTION INSURES THAT AMPLITUDE IS COMPUTED BASED ON THE GAIN SETTING THAT WAS PRESENT DURING THE LAST CYCLE OF ANALYSIS.

AS GAIN IS CHANGED, AFTER 'READ' IS OVER (OR THE OUTPUT AMPLIFIERS HAVE RETURNED TO 'HOLD'), THE NEW GAIN SETTING FOR THE NEXT CYCLE OF ANALYSIS DOES NOT EFFECT THE OUTPUT UNTIL THAT CYCLE OF ANALYSIS IS COMPLETED.

THE TWO DB AMP CH#2 AND DB AMP CH#1 ARE SUBTRACTED IN AMP 5 TO GIVE AMPLITUDE RATIO IN DB. THE SCALING REMAINS 2 VOLT/20 DB. ZERO VOLTS IS A RATIO OF 1/1. AS BOTH INPUTS ARE FOLLOWING A 'READ-HOLD' COMMAND, A5 DOES NOT REQUIRE SWITCHING ACTION.

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4.8 - AUTOMATIC GAIN CONTROL -

REFERENCE: BLOCK DIAGRAM - FIG. 4.8-1

4.8.1 - PURPOSE

THE AUTOMATIC GAIN CONTROL SYSTEM OPERATES TO KEEP EACH CHANNEL OF SIGNAL ANALYSIS AT THE CORRECT SENSITIVITY (VOLTS/VOLT OF INPUT AMPLIFIER GAIN), FOR ACCURATE ANALYSIS OF THE RETURN SIGNAL.

4.8.2 - SIGNAL UNDERLOAD & SIGNAL OVERLOAD

IF THE SIGNAL CONTENT (FUNDAMENTAL COMPONENT) OF THE RETURN SIGNAL IS TOO LOW, THE AUTOMATIC GAIN CONTROL INCREASES THE GAIN FOR THE NEXT CYCLE OF ANALYSIS. THIS IS AN 'UNDERLOAD CONDITION', AND OCCURS WHEN THE SIGNAL IS LESS THAN 25% OF FULL SCALE.

IF THE SIGNAL (FUNDAMENTAL COMPONENT) CONTENT OF THE RETURN SIGNAL IS TOO HIGH, THE AUTOMATIC GAIN CONTROL DECREASES THE GAIN FOR THE NEXT CYCLE OF ANALYSIS. THIS IS AN 'OVERLOAD (SIGNAL)' CONDITION AND OCCURS WHEN THE SIGNAL IS GREATER THAN 100% OF RANGE.

ALL GAIN CHANGES ARE BY A FACTOR OF 2, (2/1, OR 1/2).

IN BOTH CASES THE RESULTS ARE READ OUT IN THE NORMAL MANNER. THE GAIN CHANGE IS MADE AT THE START OF THE 'RESET' PERIOD, ALLOWING THE ANALYZER TO SETTLE OUT DURING THE REMAINDER OF THE RESET PERIOD FOR THE NEXT CYCLE OF ANALYSIS AT THE NEW GAIN.

DURING A SWEEP AND PLOT, THE ANALYZER NEVER GETS VERY FAR INTO THE OVERLOAD REGION OR THE UNDERLOAD REGION BEFORE A GAIN CHANGE BRINGS IT BACK INTO THE DESIRED OPERATING RANGE.

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4.8.3 - NOISE OVERLOAD

IN CONDITIONS WHERE NOISE AND HARMONICS ARE LARGE, A SECOND OVERLOAD CAN BE TRIGGERED. THIS IS REFERRED TO AS THE 'NOISE' OVERLOAD. NOISE OVERLOAD OCCURS WHEN THE INPUT AMPLIFIER AND MULTIPLIER ARE BEING DRIVEN INTO A NONLINEAR RANGE OR OPERATION. AT FULL SCALE SIGNAL, NOISE OVERLOAD OCCURS AT NOISE = SIGNAL. AT 25% FULL SCALE, NOISE = 7 X SIGNAL FOR NOISE OVERLOAD TO OCCUR.

NOISE OVERLOAD CAUSES AN IMMEDIATE ACTION. THE CYCLE OF ANALYSIS IS ABORTED BY PUTTING THE ANALYZER INTO 'RESET'. IF NOISE OVERLOAD OCCURS DURING 'HOLD', THE COMPUTATION OF PHASE SHIFT, A.R., ETC., IS COMPLETED AND ENTERED INTO THE OUTPUTS. THE NOISE OVERLOAD DID NOT EFFECT THE DATA BEING ANALYZED. THE GAIN IS REDUCED BY 1/2, AND A NEW CYCLE OF ANALYSIS IS ALLOWED TO START IN THE NORMAL FASHION.

A CONDITION OCCURS WHEN NOISE IS MUCH LARGER THAN SIGNAL, WHERE THE GAIN INCREASE TO CORRECT AN UNDERLOAD, CAUSES AN OVERLOAD. THE ANALYZER HAS JUST ENTERED 'RESET' WHEN THE UNDERLOAD IS NOTED AND THE GAIN IS INCREASED 2/1. THE NOISE CAUSES A NOISE OVERLOAD. THE GAIN IS REDUCED BY 1/2 AND OPERATION CONTINUES AT THE LOWER GAIN.

AT THE END OF EACH CYCLE OF ANALYSIS, THE PROCEDURE IS REPEATED UNTIL THE SIGNAL-TO-NOISE IMPROVES AND PERMITS THE HIGHER GAIN WITHOUT OVERLOAD. IN THE MEANTIME, THE BEST ANSWER POSSIBLE IS GENERATED AND READ OUT. THE UNDERLOAD LIGHT REMAINS 'ON', AND THE OVERLOAD LIGHT FLICKERS 'ON' AT THE END OF EACH ANALYSIS CYCLE. OPERATION WILL CONTINUE AT S/N = 1/10, AND UNDER MOST CONDITIONS GOOD RESULTS CAN BE READ OUT AND PLOTTED. OF COURSE, THE OPERATOR MUST VERIFY THAT THE NOISE IS EXPECTED AND A SIGNIFICANT FACTOR IN THE TEST.

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4.8.4 - SIMULTANEOUS NOISE OVERLOAD WITH EITHER SIGNAL UNDERLOAD OR SIGNAL OVERLOAD

THE MODEL 916 HAS BEEN DESIGNED TO PERFORM ACCURATE FREQUENCY RESPONSE MEASUREMENTS. ALLOWING THE INPUT AMPLIFIER TO NOISE OVERLOAD INTRODUCES A POTENTIALLY SERIOUS SOURCE OF ERROR. THE WAVESHAPE BEING ANALYZED IS NO LONGER THE WAVESHAPE GENERATED BY THE ITEM-UNDER-TEST. THEREFORE, PRIORITY IS GIVEN TO INTERRUPTING A CYCLE-OF-ANALYSIS WHEN A NOISE OVERLOAD OCCURS TO LOWER THE GAIN AND START A NEW CYCLE OF ANALYSIS.

TWO CONDITIONS MAY EXIST IN THE ANALYZER WHEN IT IS PUT INTO 'RESET' BY THE NOISE OVERLOAD CONDITION. THE PREVIOUS COMPLETED CYCLE OF ANALYSIS MAY HAVE HAD A SIGNAL OVERLOAD OR A SIGNAL UNDERLOAD. IF SO, THAT CONDITION STILL EXISTS AS NO NEW RESULTS HAVE BEEN ENTERED INTO THE OUTPUT BY THE NOISE ABORTED (INCOMPLETE) CYCLE OF ANALYSIS.

THUS CIRCUITRY IS INCLUDED WHICH INHIBITS THE GENERATION OF THE AUTOMATIC GAIN CONTROL 'RESET' PULSE BY THE NOISE OVERLOAD CONDITION. IT IS THIS 'AUTOMATIC GAIN CONTROL RESET' MODE WHICH NORMALLY TRIGGERS THE SIGNAL OVERLOAD AND UNDERLOAD GAIN CHANGE RESPONSE. WHEN THIS PULSE IS INHIBITED, THE NOISE OVERLOAD CAUSING A CYCLE OF ANALYSIS TO BE CUT SHORT, AND A GAIN REDUCTION OF 1/2 TO BE MADE; DOES NOT RELEASE AN UNWANTED SIGNAL OVERLOAD OR UNDERLOAD GAIN CHANGE.

THE AUTOMATIC GAIN CONTROL SYSTEM IS THEREFORE ABLE TO FUNCTION UNDER VERY SEVERE NOISE CONDITIONS AND YET RAPIDLY PRODUCE THE BEST RESULTS POSSIBLE SHORT OF THE OPERATOR USING EXTERNAL MEANS (SEE SEC. 3.4.6), SUCH AS MATCHED FILTERS, TO IMPROVE THE SIGNAL-TO-NOISE CONDITION.

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4.8.5 - CONTROLS

THE APPLICATION OF THE AUTOMATIC GAIN CONTROL IS GREATLY SIMPLIFIED AND SPEEDED UP BY THE CONTROLS AND INDICATIONS THAT ARE INCLUDED ON THE FRONT AND REAR PANELS.

THE FRONT PANEL 'PRESET GAIN' (S10) SWITCH, PUTS BOTH INPUT AMPLIFIERS INTO A HIGH GAIN CONDITION (256 V/V). THE AUTOMATIC GAIN CONTROL SYSTEM FINDS THE DESIRED OPERATING GAIN BY CORRECTING FOR A NOISE OVERLOAD (SIGNAL EXCEEDS NOISE OVERLOAD SETTING), AND SWITCHES ON DOWN TO THE CORRECT SETTING WITHOUT WAITING FOR A CYCLE OF ANALYSIS TO END. AS THE SWITCH IS RELEASED, THE CORRECT GAIN IS ESTABLISHED RAPIDLY COMPARED TO THE FREQUENCY OF OPERATION.

IF THE FREQUENCY RESPONSE TESTS ARE STARTED AT A LOW FREQUENCY, THIS GREATLY SPEEDS UP REACHING THE DESIRED GAIN SETTING.

THE FRONT PANEL CH#1 AND CH#2 OVERLOAD AND UNDERLOAD LIGHTS REFLECT THE CONDITION OF THE AUTOMATIC GAIN CONTROL. UNDER-LOAD LIGHT INDICATES SIGNAL UNDERLOAD. THE OVERLOAD LIGHTS INDICATE BOTH SIGNAL OVERLOAD AND NOISE OVERLOAD. THE SIGNAL OVERLOAD WILL CONTINUE FOR ONE CYCLE OF THE ANALYSIS TIME. NOISE OVERLOAD WILL NORMALLY FLICKER ON AND OFF AS THE NOISE OVERLOAD COMES AND GOES.

THE BACK PANEL S-20, WHEN HELD DOWN, MAKES BOTH CHANNELS GAIN = 1 VOLT/VOLTS, OR 10 VOLT INPUT FOR FULL SCALE OUTPUT. THIS IS USED FOR CALIBRATION PURPOSES. IT REMOVES THE AUTOMATIC GAIN CONTROL SYSTEM FROM THE CALIBRATION.

THE AUTOMATIC GAIN CONTROL SYSTEM IS CONTAINED ON BOARD #5, AND USES THE SIGNAL OVERLOAD AND UNDERLOAD DETERMINATIONS FROM BOARD #12. THE AMPLIFIERS BEING GAIN CONTROLLED ARE BOARDS #3 AND #4.

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4.8.6 - NOTES ON AUTOMATIC GAIN CONTROL MECHANIZATION

1) SIGNAL UNDERLOAD AND OVERLOAD DETECTION

BOARD #12 HAS THE COMPARATORS THAT SENSE SIGNAL OVERLOAD AND UNDERLOAD FOR BOTH CH#1 AND CH#2. THE AMPLITUDE COMPUTED BY THE PHASE AND AMPLITUDE CIRCUIT IS THE INPUT. THE AMPLITUDE IS UPGRADED DURING THE 'HOLD' CYCLE.

2) LOGIC FOR SIGNAL OVERLOAD RESPONSE

THE GAIN IS REDUCED AT THE START OF THE 'RESET' PERIOD IF AN OVERLOAD IS PRESENT, AND IF THE GAIN IS NOT ALREADY AT ITS LOWEST SETTING. THE CARRY OUTPUT GOES TO -15 VOLTS WHEN THE COUNT IS 0000 AND A COUNT DOWN COMMAND IS RECEIVED (LOWER COUNT = LOWER GAIN). IT BLOCKS THE CLOCK PULSE.

THUS, MORE THAN 10 VOLT SIGNAL CONTENT WILL CAUSE AN OVERLOAD THAT IS UNCORRECTABLE.

3) LOGIC FOR SIGNAL UNDERLOAD RESPONSE

THE GAIN IS INCREASED AT THE START OF THE 'RESET' PERIOD IF AN UNDERLOAD IS PRESENT.

THE RESET PULSE TRIGGERS A ONE-SHOT THAT CAUSES THE COUNTER TO BE SET TO COUNT 'UP'.

THE CLOCK PULSE IS DELAYED BY R2 C2 BY ENOUGH TO INSURE THAT UL4 IS SET UP FOR COUNT 'UP'. THE COUNTER INCREMENTS ONE COUNT UP AND THE GAIN IS INCREASED 'X2'.

WHEN THE COUNT REACHES 1010 (GAIN = 1024 VOLTS/VOLT), A $\overline{\text{HIGH}}$ $\overline{\text{COUNT}}$ INPUT FROM THE INPUT AMPLIFIER BLOCKS THE RESET PULSE. THE COUNTER IS NOT CHANGED. THE INPUT AMPLIFIER IS AT MAXIMUM GAIN, AND THE SIGNAL IS UNDER 4 MV PEAK. THE UNDERLOAD LIGHT IS 'ON' AND REMAINS ON.

4) 'SIGNAL + NOISE' OVERLOAD

THE FULL OUTPUT OF THE INPUT AMPLIFIER IS ANOTHER INPUT TO BOARD #5. AN OVERLOAD DETECTOR TRIGGERS A ONE-SHOT WHEN THE NOISE EXCEEDS ±10 VOLTS. THIS, IN TURN, CLOCKS THE COUNTER DOWN ONE COUNT, AND 'RESET' THE NOISE COMPARATOR.

IF THE NOISE IS LARGE ENOUGH, (AS DURING A STARTUP), THE RELEASE OF THE ONE-SHOT, WILL FIND THAT THE INPUT AMPLIFIER (AT A GAIN OF 1/2 OF ITS ORIGINAL GAIN) STILL CAUSES THE NOISE OVERLOAD DETECTOR TO FIRE THE ONE-SHOT.

THE GAIN IS THUS DROPPED IN RAPID STEPS OF 'X 1/2' UNTIL A GAIN IS REACHED WHERE THE NOISE OVERLOAD DETECTOR NO LONGER SENSES AN OVERLOAD.

THE NOISE OVERLOAD RESPONSE OF THE AUTOMATIC GAIN CONTROL IS INTERLOCKED WITH 0000. IT CANNOT REDUCE THE GAIN BELOW 1 VOLTS/VOLT (10 VOLT F.S. SENSITIVITY). THE CARRY OUTPUT OF THE COUNTER IS USED EXACTLY AS FOR SIGNAL OVERLOAD.

THE NOISE ONE-SHOT CANNOT BE FIRED DURING THE "HOLD" AND "RESET" MODES OF THE ANALYZER. THIS PREVENTS GAIN CHANGE WHEN A NEW RESULT IS BEING READ INTO THE OUTPUT (HOLD), AND PREVENTS THE INPUT AMPLIFIER TRANSIENTS FOLLOWING A SIGNAL OVERLOAD OR SIGNAL UNDERLOAD GAIN CHANGE (DURING RESET) FROM TRIGGERING A FALSE NOISE OVERLOAD.

MODEL 916-TWO CHANNEL SWEEP FREQUENCY RESPONSE ANALYZER

Block Diagram

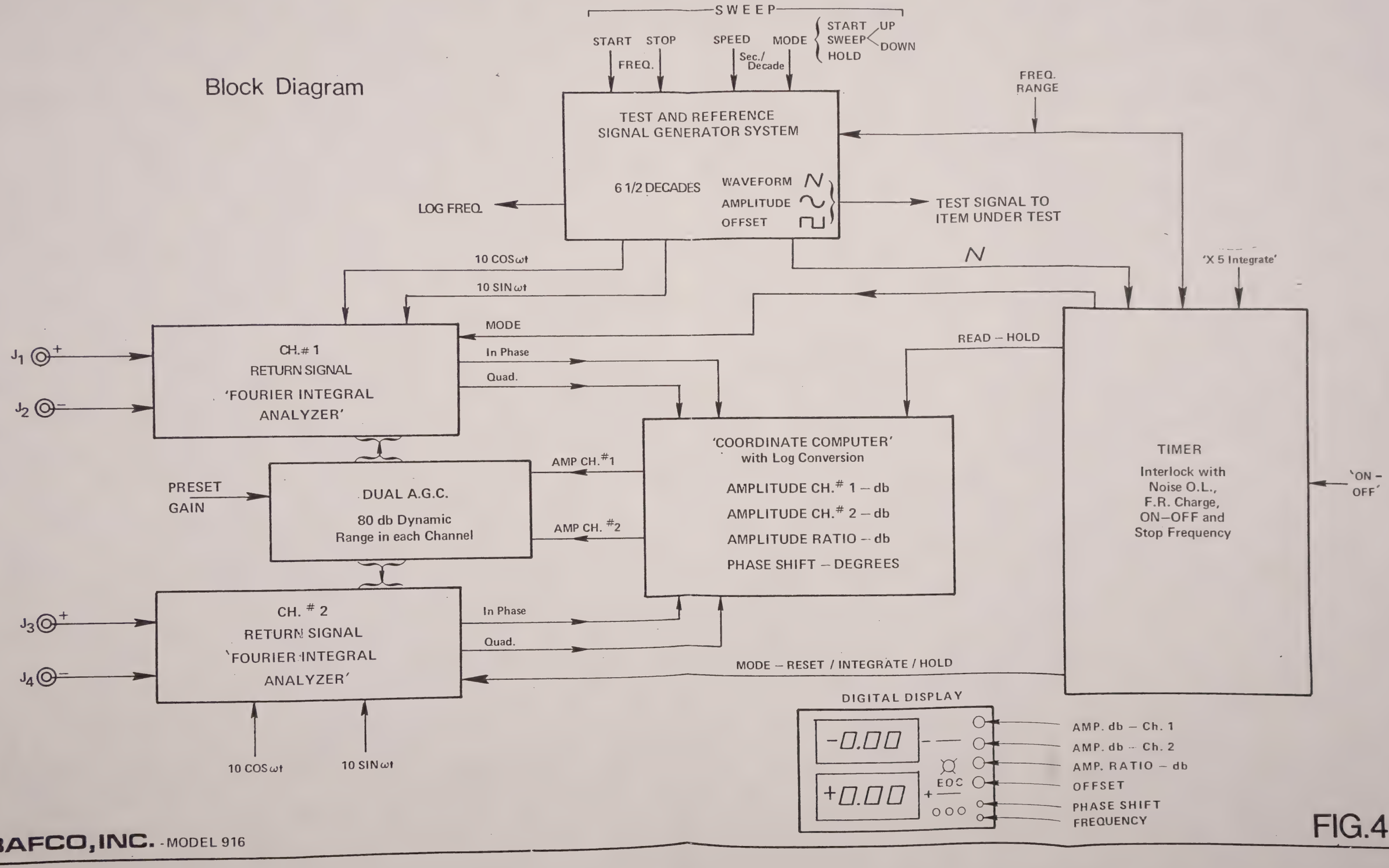


FIG.4-1

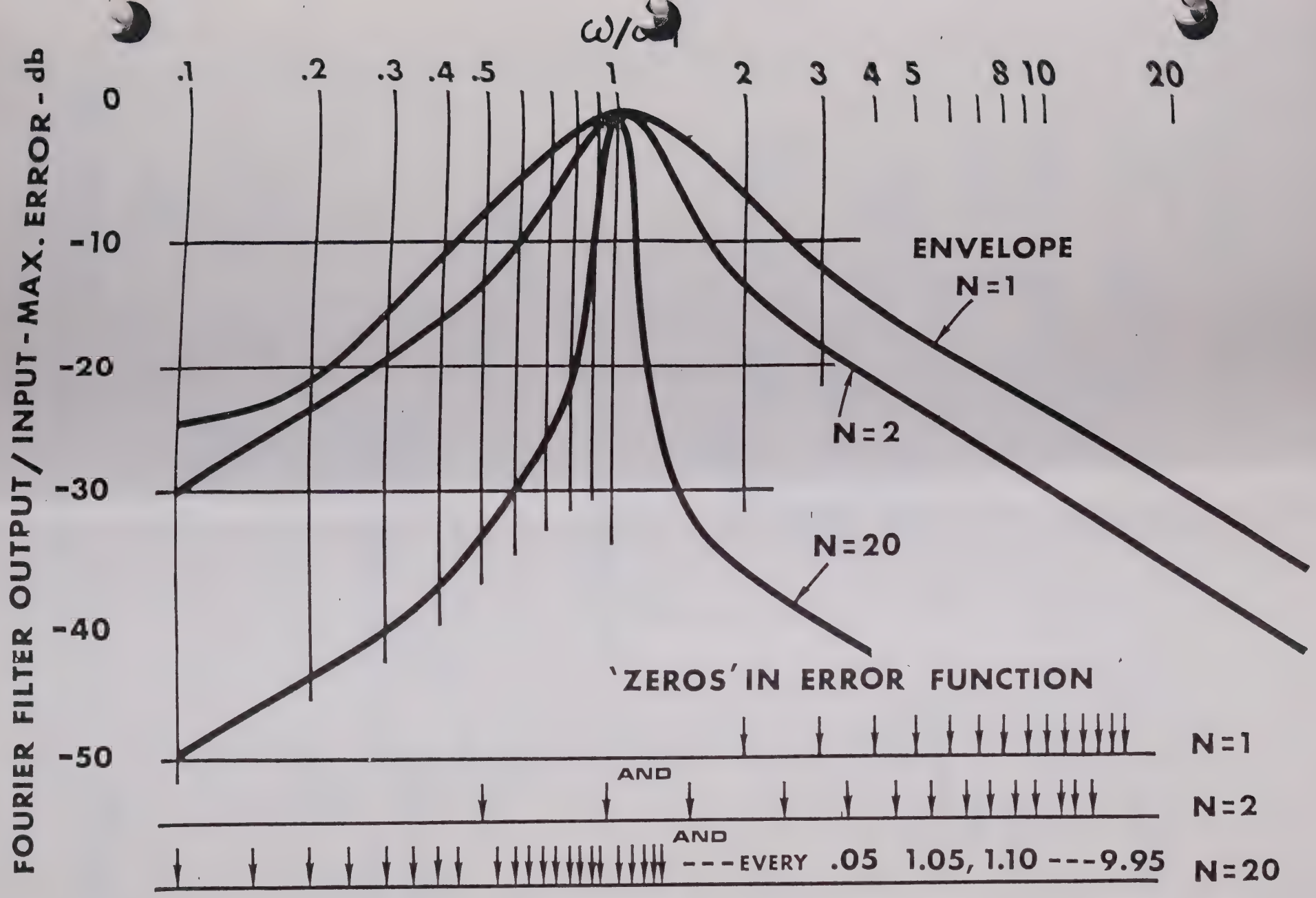


FIG.4.2-1 **MAXIMUM ERROR IN FOURIER FILTER RESPONSE VS NOISE FREQUENCY / TEST FREQUENCY**

FREQUENCY SWEEP SYSTEM

Simplified Block Diagram

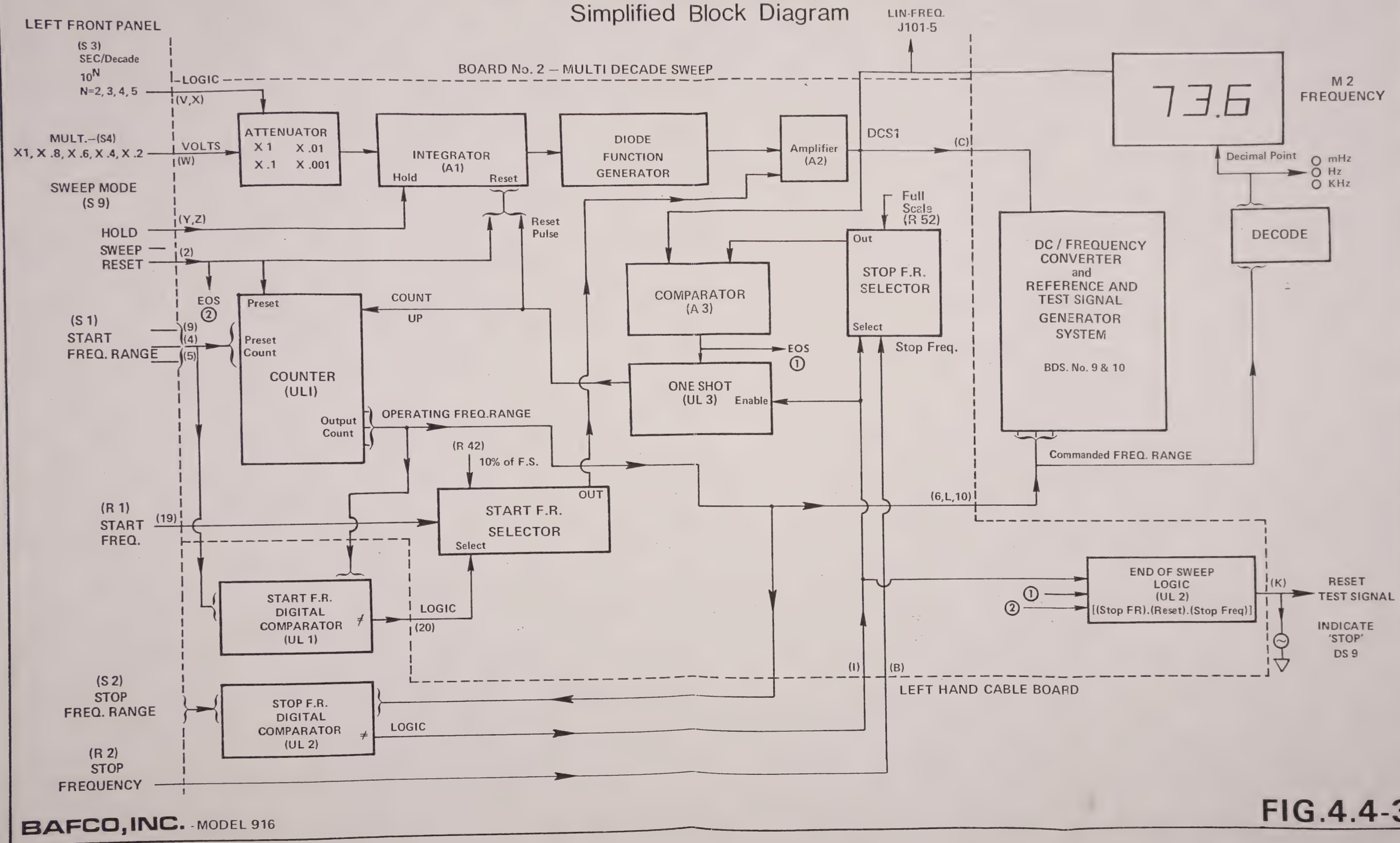
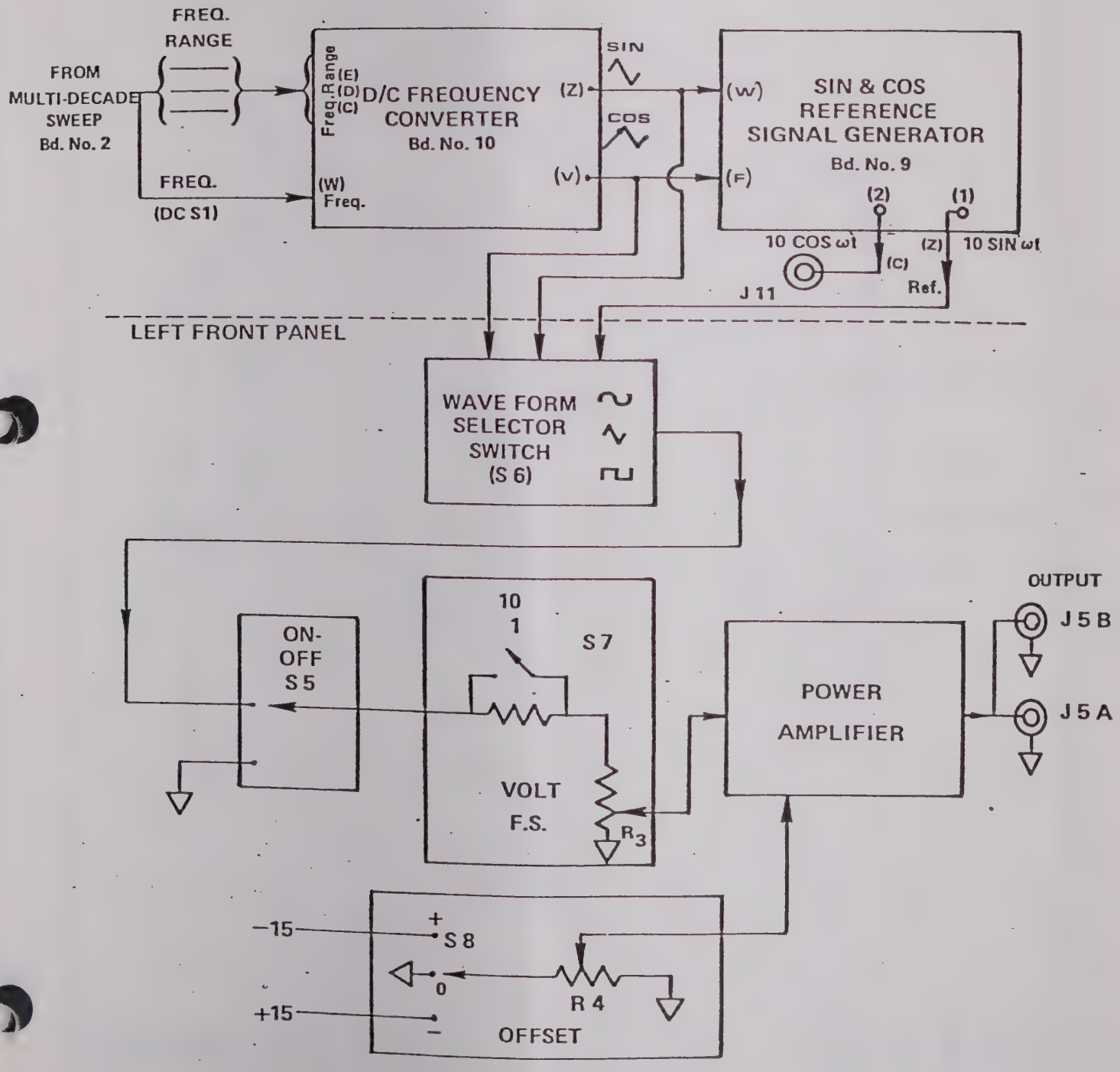


FIG.4.4-3

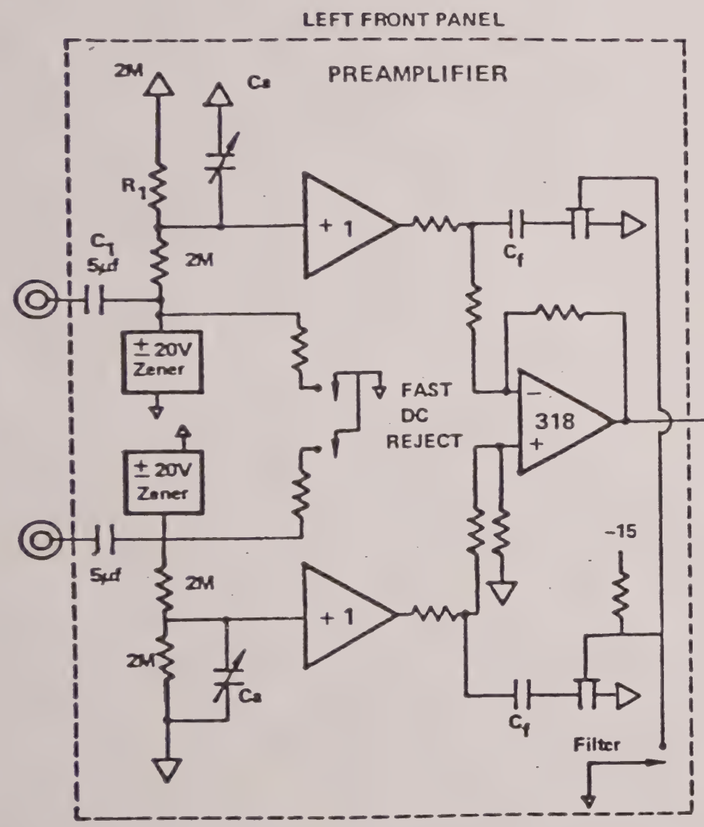
REFERENCE AND TEST SIGNAL GENERATOR SYSTEM

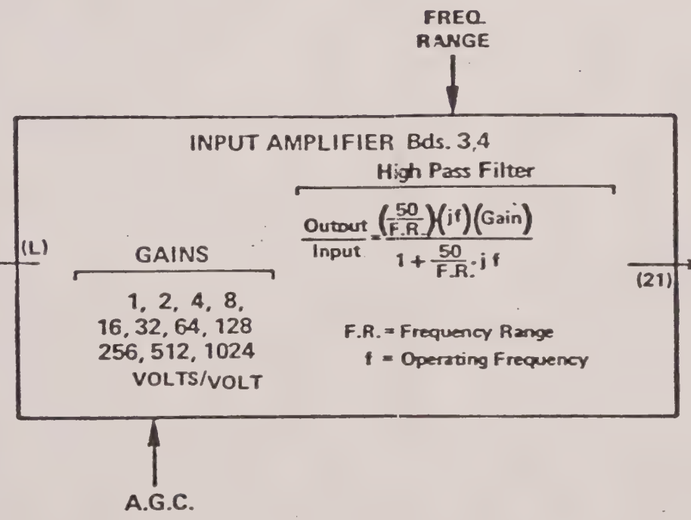
BLOCK DIAGRAM



RETURN SIGNAL

Input Preamplifier, Input Amplifier, Multiplier,
Attenuator & Integrator





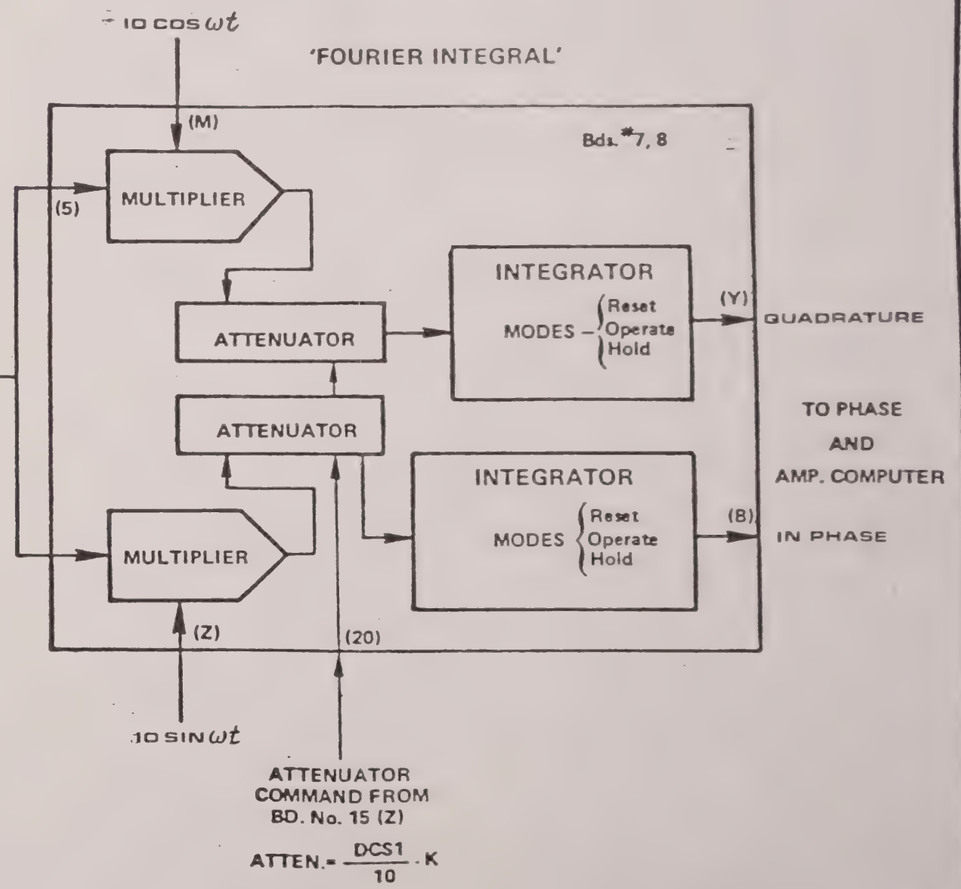
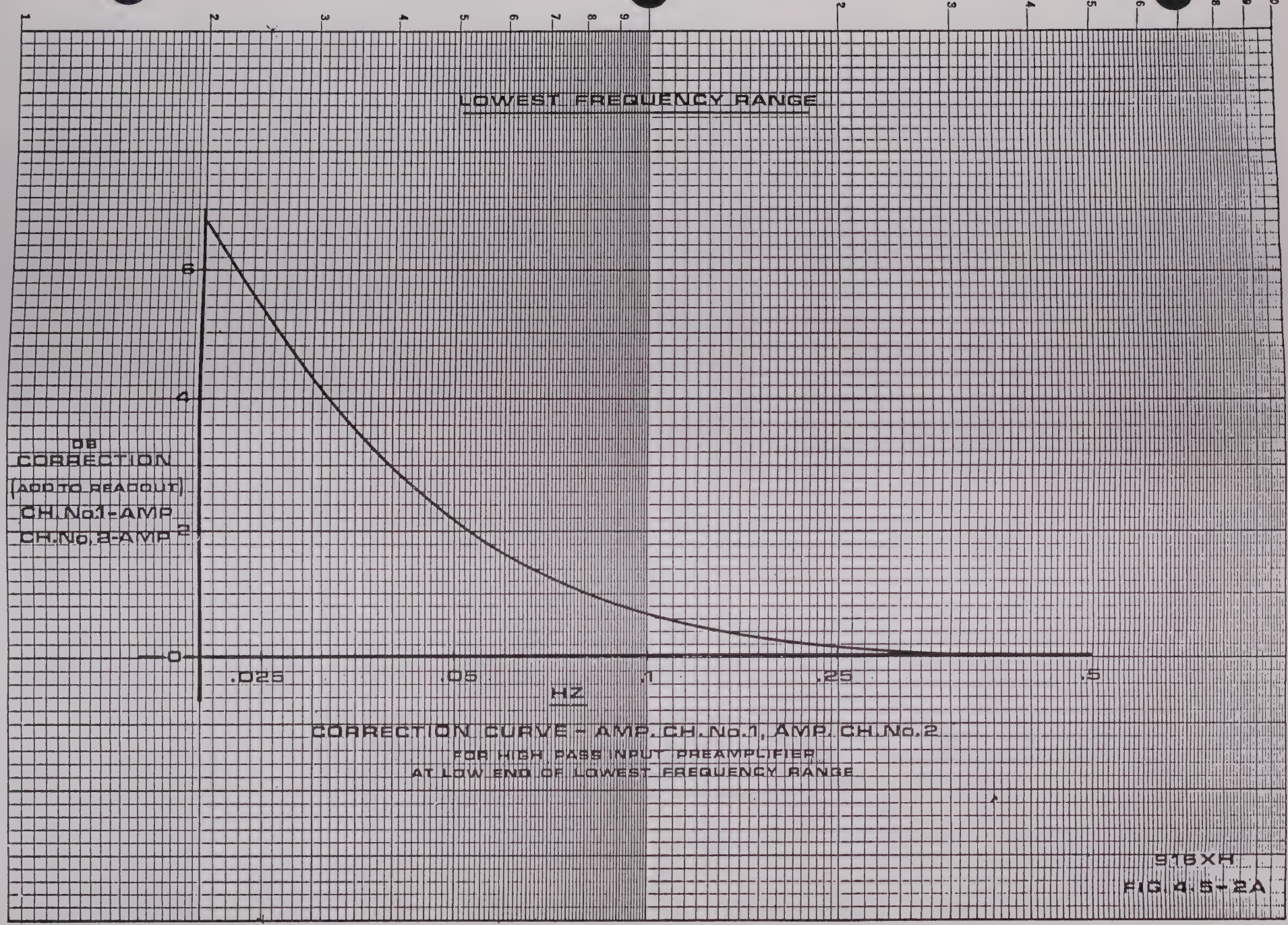


FIG.4.5-1

K&E SEMI-LOGARITHMIC
2 CYCLES X 70 DIVISIONS MADE IN U.S.A.
KEUFFEL & ESSER CO.



CORRECTION CURVE - AMP. CH. No. 1, AMP. CH. No. 2
FOR HIGH PASS INPUT PREAMPLIFIER
AT LOW END OF LOWEST FREQUENCY RANGE

9.16XH
FIG. 9.5-2A

K&E SEMI-LOGARITHMIC 46 4973
2 CYCLES X 70 DIVISIONS MADE IN U.S.A.
KEUFFEL & ESSER CO.

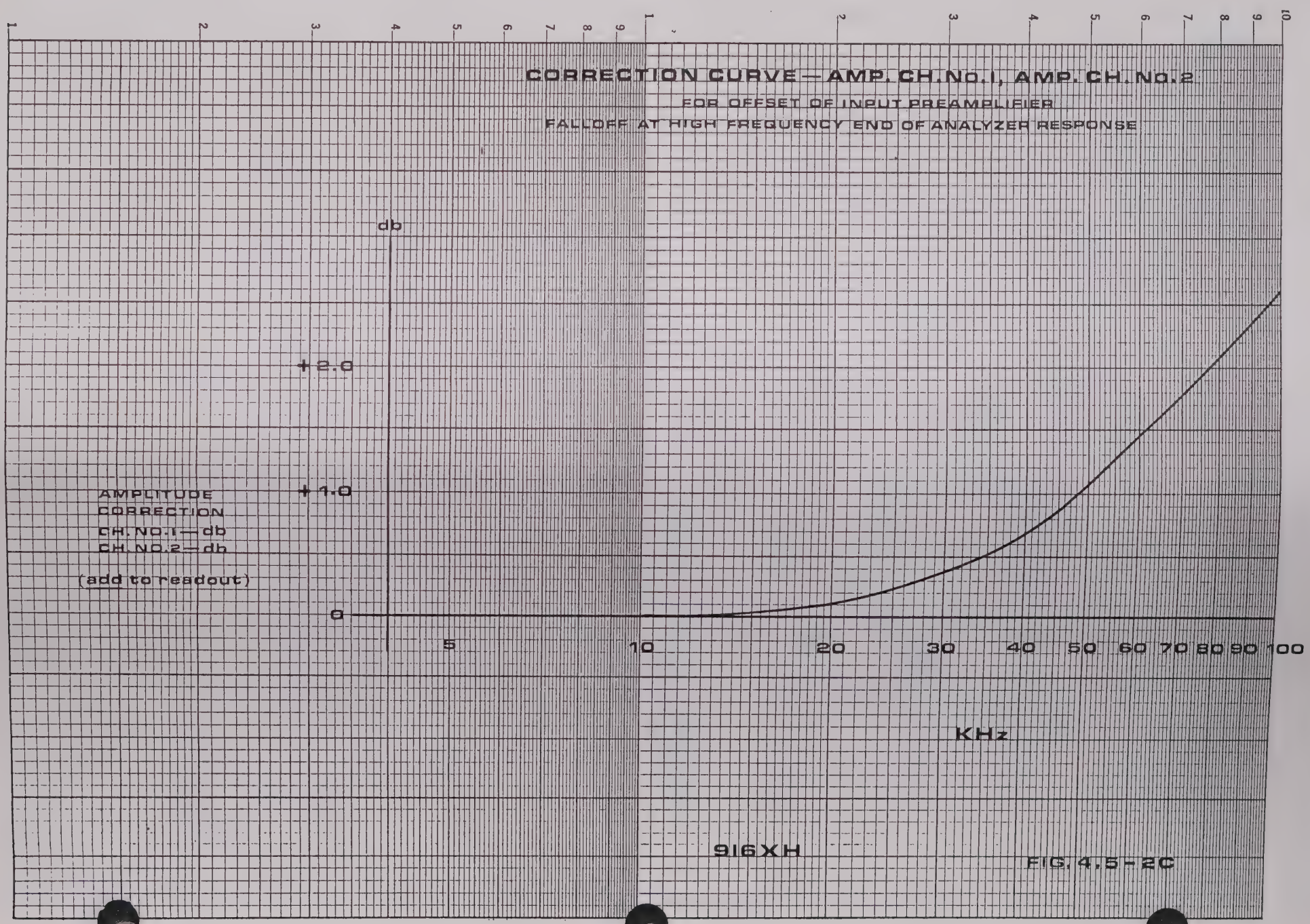


FIG. 4.5-2C

TIMING SYSTEM

Block Diagram (Bd.#16)

TEST FREQUENCY

PULSE GENERATOR
Four per Cycle (ULI)

439 hz

F.R. (1+2+3+4)

SELECTOR LOGIC

F.R. (5+6)

X 5

FREQ. RANGE

PULSE COUNTER

FULL SCALE HZ	X5	PULSE COUNT	X5	PULSE COUNT
.1	OUT	4	IN	8
1.0	OUT	4	IN	8
10.	OUT	8	IN	40
.1K	OUT	80	IN	400
1K	OUT	80	IN	400
10K	OUT	80	IN	400

HOLD ONE SHOT 'A'

R

C

AND –1–

(22) READ–HOLD (To Amp.,Phase) (Output Circuits)

(M) INTEGRATOR HOLD

RESET COUNTERS

SET

Inhibit

TRIGGER DELAY

RESET FLIP–FLOP

MINIMUM RESET TIME ONE–SHOT

INPUT

ON-OFF (S)

END-OF-SWEEP (K)

AND –2–

RESET

Logic for Decision 'Start a New Cycle of Analysis'

(L) RESET INTEGRATORS

INPUT

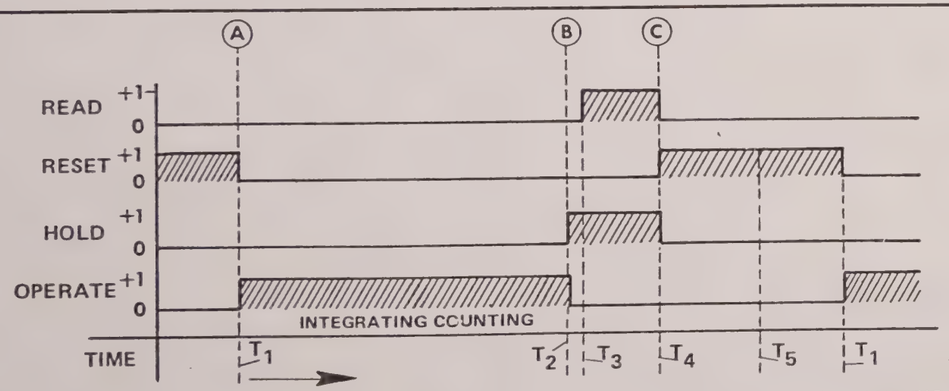
INTERLOCK PULSE GENERATOR

(X) NOISE O.L.

(Y) FREQ. RANGE CHANGE

ON-OFF

(Z) EXTERNAL

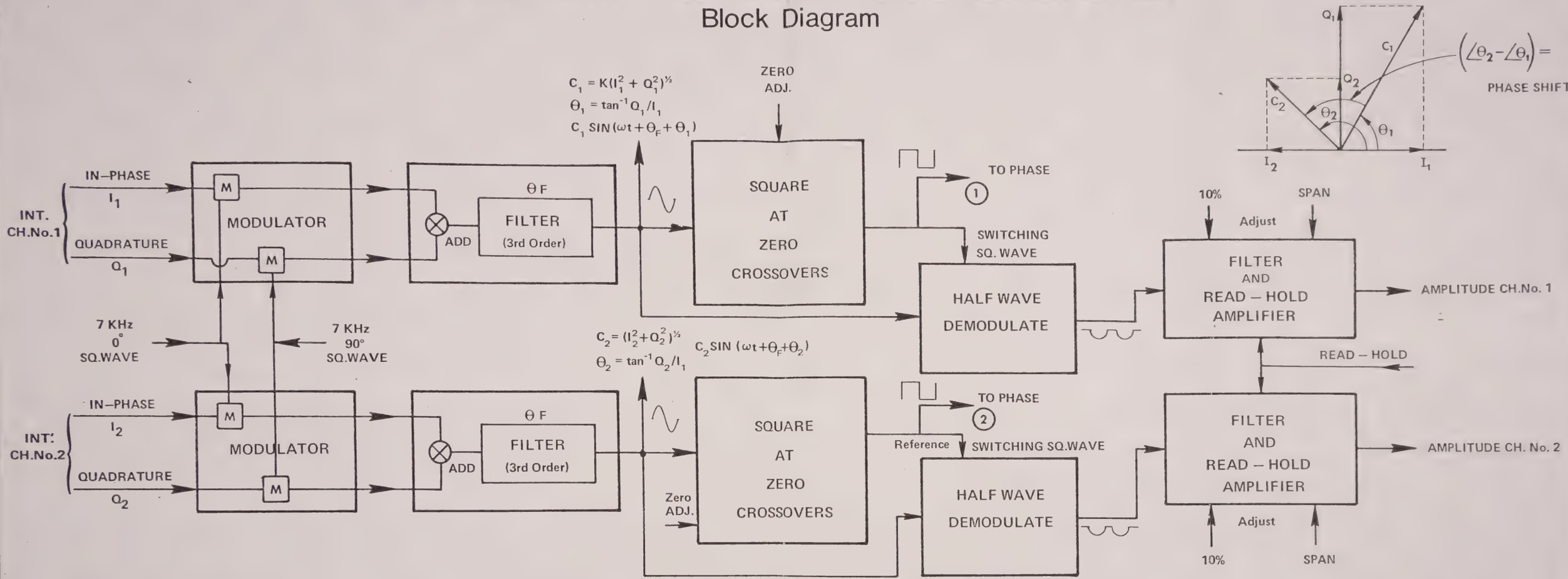


T_1 –A– MIN. RESET TIME COMPLETED AND FIRST PULSE THRU 'AND 2' GATE.
T_2 –B– COUNT COMPLETE, HOLD ONE–SHOT TURNED 'ON'.
T_3 – DELAYED COMMAND TO 'READ' NEW RESULTS OF PHASE AND AMPLITUDE.
T_4 – END OF HOLD AND OF READ, START OF RESET.
T_5 – MINIMUM RESET TIME,etc.

FIG.4.6-1

PHASE SHIFT & AMPLITUDE COMPUTER

Block Diagram



PHASE

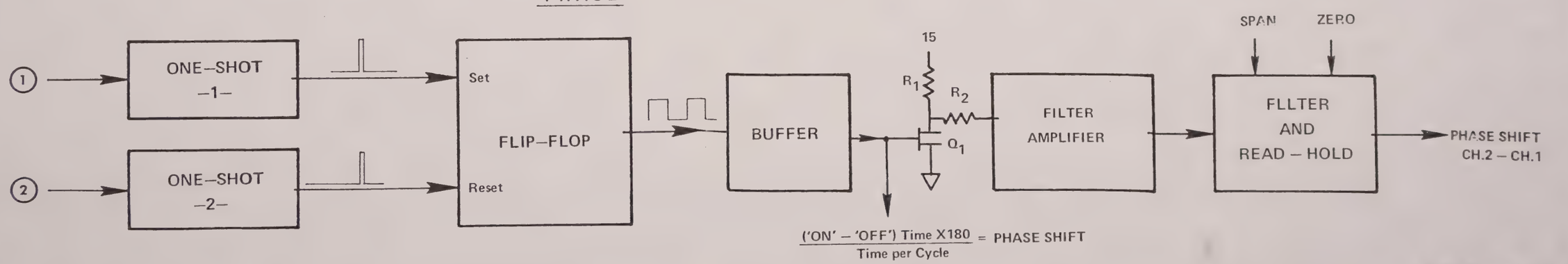


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FIG.4.7-1

AMPLITUDE - db ; AMPLITUDE RATIO (db)

Block Diagram

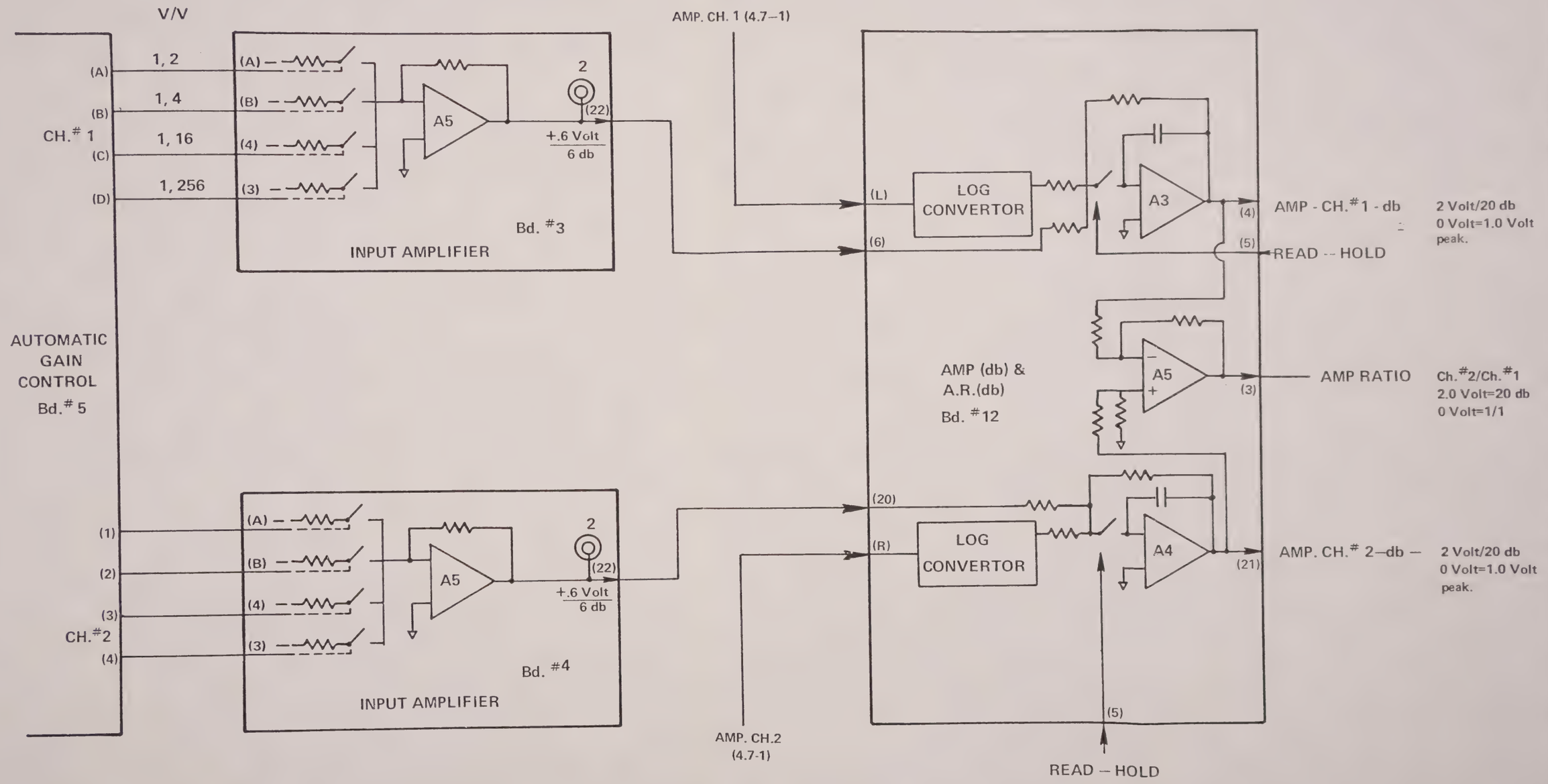

FIG.4.7-2

AUTOMATIC GAIN CONTROL

Block Diagram - Shown for One Channel (#1)

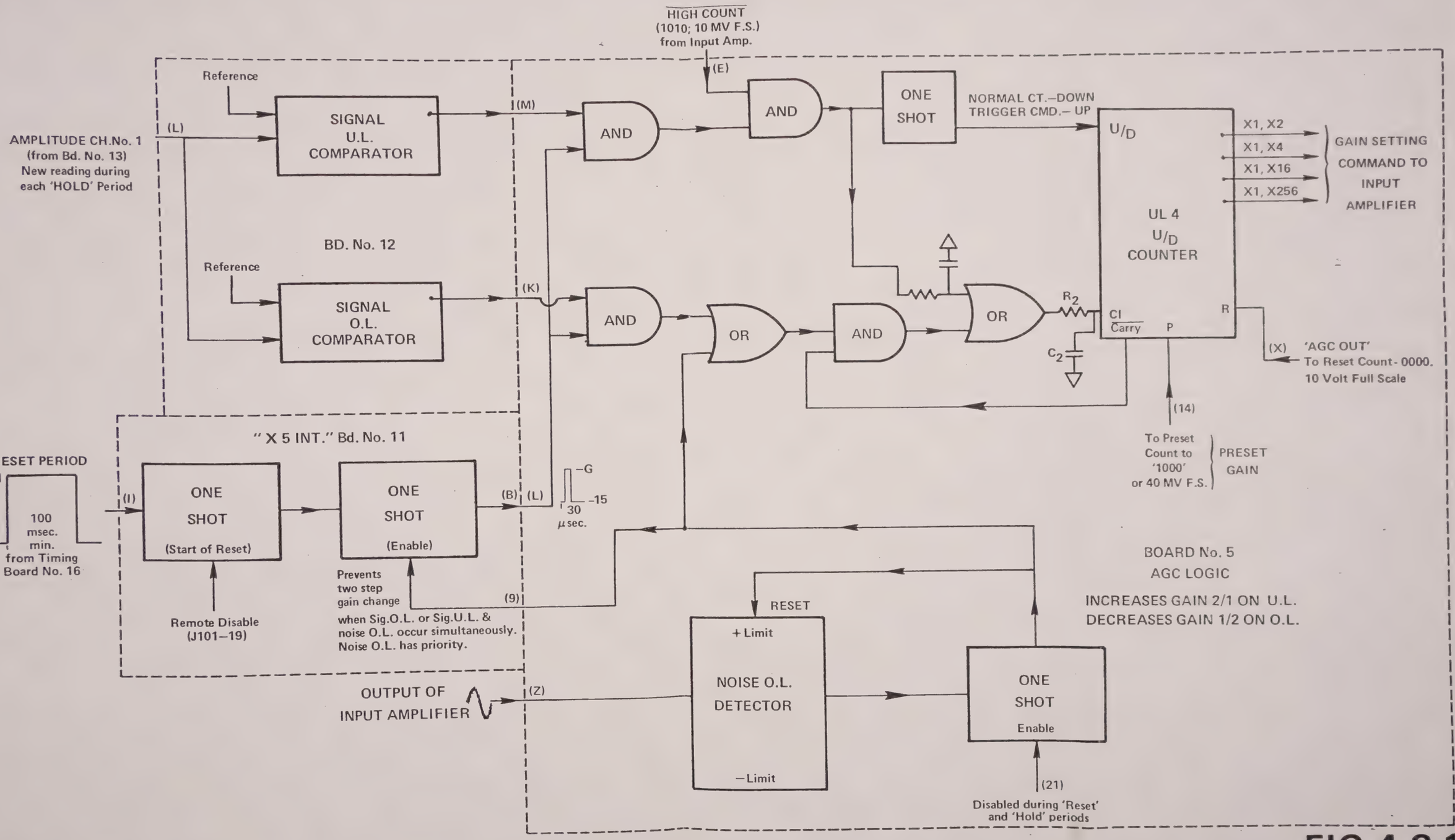

FIG.4.8-1

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5 - INDIVIDUAL CIRCUIT BOARDS

5.1 - LEFT FRONT PANEL & CABLE BOARDS - INPUT PREAMPLIFIER, OUTPUT AMPLIFIER

5.1.1 - LEFT FRONT PANEL & CABLE BOARD

REFERENCE: DRAWING NO. C102992-1

S1-UL1 - START FREQUENCY RANGE

S1 HAS THREE OUTPUT LINES WHICH COMMAND THE START FREQUENCY RANGE. PIN 'X' = ALT, PIN 'W' = (3 + 4), PIN 'Y' (5 + 6), CODED AS:

FREQUENCY RANGE			PINS		
FULL SCALE		NO.	'Y'	'W'	'X'
1	HZ	1	0	0	0
10	HZ	2	0	0	1
100	HZ	3	0	1	0
1000	HZ	4	0	1	1
10	KHZ	5	1	0	0
100	KHZ	6	1	0	1

THESE LINES ARE THE COMMAND TO THE EXTENDED SWEEP BOARD #2, START FREQUENCY RANGE.

UL1 COMPARES THE START FREQUENCY RANGE WITH THE ACTUAL FREQUENCY RANGE. ITS OUTPUT LOGIC LEVEL IS PLUS AT PIN 'S' WHEN THEY AGREE, AND '0' WHEN THE SWEEP ADVANCES TO THE NEXT AND SUCCEEDING FREQUENCY RANGES.

S2-UL2 - STOP FREQUENCY RANGE

S2 SETS THE STOP FREQUENCY RANGE WITH THE SAME CODING AS THE START (S1 ABOVE) AS THE THREE LINE INPUT TO COMPARATOR UL2.

UL2 COMPARES THE COMMANDED STOP FREQUENCY RANGE WITH THE ACTUAL FREQUENCY RANGE (FROM EXTENDED SWEEP BOARD TO PINS 'V', 'U', AND 'P' OF LEFT HAND CABLE. ITS OUTPUT TO PIN 'R' IS 'PLUS' WHEN THE FREQUENCY RANGE OF OPERATION REACHES THE STOP FREQUENCY RANGE ANS IS 'ZERO' AT ALL OTHER TIMES.

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R1, R57 - START FREQUENCY

R1 SETS THE DC VOLTAGE THAT COMMANDS THE 'START' FREQUENCY (WITHIN THE FREQUENCY RANGE). R57 SCALES THE OUTPUT TO -10.0 VOLTS FULL SCALE. R1 IS A LINEAR 10 TURN POT WITH DIRECT READING DUAL READOUT.

R2, R58 - STOP FREQUENCY

R2 SETS THE DC VOLTAGE THAT COMMANDS THE 'STOP' FREQUENCY OF THE SWEEP WITHIN THE STOP FREQUENCY RANGE.

R58 SCALES FULL SCALE TO -10.0 VOLTS.

DS5, Q3 - O.L., CH#1
DS7, Q4 - O.L., CH#2

Q3 DRIVES DS5, AND Q4 DRIVES DS7. WHEN THE INPUT IS AT GROUND, THE LIGHTS ARE DEENERGIZED. WHEN THE INPUT (PIN 'L' FOR CH#1, PIN 'N' FOR CH#2) GOES TO -15 VOLTS, THE RESPECTIVE LIGHT IS ENERGIZED. THUS, THE COMMAND IS OL.

DS4, DS6, - U.L. CH#1, U.L. CH#2

THE UL LIGHTS ARE DRIVEN DIRECTLY. WHEN THE INPUT (PIN '14' - CH#1, PIN 'M' - CH#2) IS AT GROUND, THE RESPECTIVE LIGHT IS ENERGIZED. THE COMMAND IS U.L.

S9, DS2, DS3, DS8, DS9, Q1, Q2
SWEEP MODE - RESET, SWEEP, HOLD

WHEN S9A-RESET IS DEPRESSED, DS8 IS ENERGIZED. PIN '13' IS GROUNDED. THUS RESET IS COMMANDED AND INDICATED.

WHEN S9B IS DEPRESSED, THE RUN LIGHT IS GROUNDED AT ITS ANODE. Q1 ACTS AS AN EMITTER FOLLOWER. AS LONG AS PIN 'K' IS AT -15 VOLTS, (STOP), THE SWEEP LIGHT IS ENERGIZED. WHEN THE STOP FREQUENCY IS REACHED, PIN 'K' GOES TO GROUND, DS2 IS DEENERGIZED, AND AND DS9 (STOP INDICATION) IS ENERGIZED.

WHEN S9C IS DEPRESSED, PIN 'E' IS DRIVEN TO -15 VOLTS, AND DS3 IS ENERGIZED THRU R18.

DS3 IS ALSO ENERGIZED BY EMITTER FOLLOWER Q2 WHEN THE $\overline{\text{HOLD}}$ LINE GOES TO -15 VOLTS. (THIS OCCURS WHEN HOLD SWEEP IS COMMANDED BY THE TIMING BOARD).

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S3 - N - 10^N SEC./DECADE

S3 - FOUR POSITION SWITCH WITH A TWO LINE OUTPUT TO PINS '18' AND '21' CODED TO COMMAND THE ATTENUATOR ON THE EXTENDED SWEEP BOARD AS:

N	FULL SCALE SEC./DECADE	18	21	
1	10	OFF	OFF	OFF = -15 VOLTS
2	100	OFF	ON	FROM BD #2,
3	1,000	ON	OFF	
4	10,000	ON	ON	ON = GROUND

S4 - 'X' - SWEEP SPEED MULTIPLIER

SELECTS D.C. VOLTAGE TO THE EXTENDED SWEEP BD#2, THRU PIN '19' AS:

'X'	+ VOLTS	
1.0	3.0	VOLTAGE INCREASE TO DECREASE - SEC. PER DECADE
.8	3.75	
.6	5.0	
.4	7.5	
.2	15.0	

S14 - DOWN

SWITCHES POLARITY OF D.C. VOLTAGE FROM S4 FROM PLUS TO MINUS. AS LONG AS IT IS HELD IN DEPRESSED POSITION, SWEEP REVERSES AND GOES DOWN IN FREQUENCY (CANNOT CHANGE FREQUENCY RANGE).

S15 - 'X5' INTEGRATE

APPLIES GROUND TO PIN '7' WHEN 'OUT', AND -15 VOLTS WHEN 'IN'. IT IS AN X5 COMMAND.

IN THE 'IN' POSITION, ANALYSIS TIME IS INCREASED 2/1 IN FREQUENCY RANGE (1 + 2) AND 5/1 IN FREQUENCY RANGES 3, 4, 5 & 6.

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5.1.2 - INPUT PREAMPLIFIERS

REFERENCE: DRAWING NO. C102992-2

THE DESCRIPTION WILL BE OF CHANNEL #1, WITH THE EQUIVALENT ITEMS OF CH#2 IN PARENTHESES.

CONNECTION

J3A, J4A - (J1A, J2A) - THESE BNC'S ARE THE BALANCED RETURN SIGNAL INPUT. IF A SINGLE ENDED RETURN SIGNAL IS USED, THE UNUSED INPUT MUST BE GROUNDED.

HIGH PASS INPUT FILTER
C10, R16, R17, A4; C16, R26, R24, A5
(C1, R4, R6, A1; C6, R34, R11, A2)

EACH RETURN SIGNAL IS A.C. COUPLED BY THE ABOVE HIGH PASS FILTER. THE TIME CONSTANT IS 20 SECONDS.

THE FOLLOWER AMPLIFIER PROVIDES A VERY HIGH INPUT IMPEDANCE. THE ATTENUATION OF THE RETURN SIGNAL BY 1/2 PERMITS A 20 VOLT PEAK INPUT WITH 10 VOLT PEAK OF SIGNAL AND 10 VOLTS OF NOISE AS A MAXIMUM.

ZENER DIODE LIMITER
CR3, 4; CR5, 6, (CR1, 2; CR3, 4)

THE INPUT CONDENSER OUTPUT IS LIMITED TO ±20 VOLTS BY THE ZENER DIODE. THIS PREVENTS DAMAGE TO THE REMAINDER OF THE CIRCUITRY WHEN APPLYING 100 VOLT D.C. TO THE INPUT.

FAST D.C. REJECT
S11, R13, R14, (S12, R1, R2)

DEPRESSING S11 (S12) CONNECTS THE INPUT CONDENSERS TO GROUND WITH A RELATIVELY LOW RESISTANCE. THIS RAPIDLY CHARGES (50 MILLISEC. TIME CONSTANT) THE CONDENSERS TO THE INPUT D.C. LEVEL RATHER THAN WAIT FOR THE 20 SECOND TIME CONSTANT. S11 (S12) ARE ONLY USED WHEN A LARGE CHANGE IN D.C. INPUT OCCURS, AS WHEN MAKING A NEW CONNECTION OR CHANGING AN OPERATING POINT.

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DOUBLE ENDED TO SINGLE ENDED AMPLIFIER
A6 (A3) & ASSOCIATED RESISTORS

A6 (A3) SUBTRACTS THE TWO INPUTS AT THE FOLLOWER OUTPUT TO GIVE THE NET INPUT SIGNAL AT PIN '4' ('20').

R29 (R36) OPTIMIZES THE SUBTRACTION TO GIVE HIGH COMMON MODE REJECTION.

INPUT FILTER - C11, C17 (C3, C7)

THESE ADJUSTABLE CONDENSERS PROVIDE AN ATTENUATION OF HIGH FREQUENCY NOISE, AND A PLACE TO EQUALIZE THE PHASE SHIFT THRU ALL FOUR INPUTS. SEE SECTION 6.11.5 FOR THE CALIBRATION PROCEDURE.

S13 - FILTER OUT-IN - Q4, Q3 C19, C14
(Q1, Q2, C9, C4)

WHEN S13 IS DEPRESSED, A LOW PASS FILTER (SINGLE POLE) IS ADDED. THE FILTER IS INTENDED TO ATTENUATE HIGH FREQUENCY NOISE. THE FILTER IS MATCHED IN THE TWO CHANNELS.

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5.1.3 - OUTPUT AMPLIFIER

S6 - WAVEFORM SELECT

S6 SELECTS SINE WAVE (PIN '6' ON L.H. CABLE), TRIANGLE WAVE (PIN 'B'), OR SQUARE WAVE (PIN '3').

S5 - OUTPUT - 'ON-OFF'

WITH S5 'OFF', THE OUTPUT OF S6 IS DISCONNECTED. THUS, THERE IS ZERO TEST SIGNAL AT THE OUTPUT. PIN 'C' IS AT GROUND. THIS RESETS THE ANALYZER AND THE D.C./FREQUENCY GENERATOR.

WITH S5 'ON', THE WAVEFORM SELECTED BY S6 IS CONNECTED TO THE OUTPUT THRU R37, R3. PIN 'C' IS AT -15 VOLTS (FROM TIMING BOARD), AND THE ANALYZER IS RETURNED TO NORMAL OPERATION.

S7 - R37, R3 - VOLTS F.S. -10., 1.0

S7A DEPRESSED SHORTS R37. THE FULL 10. VOLT PEAK SIGNALS ARE ACROSS R3 AND BECOME AVAILABLE AT THE OUTPUT.

S7B DEPRESSED ATTENUATES THE INPUT TO R3 TO 1.0 VOLT PEAK AND SETS FULL SCALE AT 1.0 VOLT PEAK AT THE OUTPUT. R3 IS THE LINEAR POT THAT SETS THE OUTPUT LEVEL. THE POT LINEARITY MAKES ITS SETTING DIRECT READING.

S8, R40, R41, R4 - OFFSET

R4 ADJUSTS THE OFFSET LEVEL. FOR S8C DEPRESSED, R4 IS DEENERGIZED. FOR S8B DEPRESSED, R4 IS ENERGIZED FROM -15 VOLTS THRU R41. R4 CONTROLS THE OUTPUT OFFSET FROM 0 TO +10 VOLTS.

FOR S8C DEPRESSED, R4 IS ENERGIZED FROM -15 VOLTS THRU R40. R4 CONTROLS THE OUTPUT OFFSET FROM 0 TO -10 VOLTS.

FOR PRECISE SETTING OF 'OFFSET', USE METER #1 AND OFFSET SWITCH.

NOTE THAT USING S5 TO TURN THE SIGNAL 'ON' OR 'OFF' DOES NOT EFFECT THE OFFSET.

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OUTPUT FOLLOWER & POWER AMPLIFIER
A7, A8, Q5, Q6

A7 IS A FOLLOWER AMPLIFIER THAT ISOLATES R3 FROM A8. IT HAS A GAIN OF +1.00 VOLTS/VOLT.

A8 IS THE OUTPUT AMPLIFIER. Q5, Q6 AND ASSOCIATED COMPONENTS BOOST THE OUTPUT TO ±30 MA AT ±10 VOLTS.

CR9, CR10 PROVIDE A BIAS TO INSURE THAT THE QUIESCENT OUTPUT CONDITION STILL REQUIRES CURRENT THRU Q5, Q6.

MISCELLANEOUS

S10 - PRESET GAIN

S10 GROUNDS PIN '15' WHEN 'PRESET GAIN' IS DEPRESSED. THIS FORCES THE INPUT AMPLIFIERS TO A 40 MV FULL SCALE SENSITIVITY. IT IS USED TO START THE A.G.C. FROM OVERLOAD CONDITION. IN THE OUT POSITION, PIN '15' IS AT -15 VOLTS (FROM A.G.C. BD#5).

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5.2 - MULTI-DECADE SWEEP - BOARD #2

REFERENCE: DRAWING NO. C102708 & SEC. 4.4.5 FOR THEORY OF OPERATION IN SWEEP, AND SEC. 4.4.2 FOR FREQUENCY OF OPERATION IN RESET.

5.2.1 - PURPOSE

THE MULTI-DECADE SWEEP BOARD IS THE MAJOR PORTION OF THE EXTENDED SWEEP SYSTEM. THEORY OF OPERATION IS GIVEN IN SEC. 4.4.5 AND REFERENCE IS MADE TO BLOCK DIAGRAM 4.4.-3.

IN FREQUENCY BY FREQUENCY TESTING, THIS BOARD SCALES DCS1 FROM R1 (FREQUENCY SETTING), AND COMMANDS ANALYZER OPERATION AT THE START FREQUENCY RANGE.

5.2.2 - SWEEP AMPLIFIER - A1

AMP #1 IS CONNECTED AS AN INTEGRATOR WITH HOLD, INTEGRATE AND RESET MODES OF OPERATION. C5 IS THE INTEGRATE CONDENSER, AND R16 IS THE INPUT RESISTOR. THEY ARE SIZED FOR A 50 SECOND INTEGRATE TIME.

THE NET INPUT TO A1 IS DETERMINED BY THE FRONT PANEL SETTINGS OF 'S3'. 10^N SECONDS/DECADE AND THE S4 MULTIPLIER SWITCHES. 'S3' CONTROLS THE ATTENUATOR MADE UP OF R10, R12, Q1, R11, R15, Q2. THE INPUT VOLTAGE IS ATTENUATED BY THE S3 SETTING AS FOLLOWS:

S3 - 10^N SEC./DECADE

N	ATTENUATION	
1	1.	
2	0.1	(Q1 'ON')
3	0.01	(Q2 'ON')
4	.001	(Q1 & Q2 'ON')

THE INPUT COMMAND TO TE 'W' IS CONTROLLED BY THE MULTIPLIER SWITCH S4 AS FOLLOWS:

S4-'X'	VOLTS - TE 'W'
.2	+15.0
.4	7.5
.6	5.0
.8	3.75
1.0	3.0

5.2 - MUTLI-DECADE SWEEP - BOARD #2

5.2.2 - SWEEP AMPLIFIER - A1 - CONT'D.

THE VOLTAGE IS INVERSELY PROPORTIONAL TO THE NET 'SEC./DECADE' MULTIPLIER SETTING (HIGHER INPUT VOLTAGE FOR LOWER SEC./DECADE).

Q3 IS 'ON' DURING SWEEP. Q3 IS 'OFF' DURING 'HOLD'. 'HOLD' IS COMMANDED BY ONE OF THE FOLLOWING:

S9C ON FRONT PANEL.
AT THE END OF SWEEP.
MOMENTARILY DURING NOISE OVERLOAD GAIN CORRECTION.
MOMENTARILY DURING FREQUENCY RANGE SWITCHING.
WHEN THE TEST SIGNAL IS TURNED 'OFF' BY 'S5'.

R20 PROVIDES AN ADJUSTABLE BIAS TO SET THE DRIFT OF A1 TO NEAR ZERO DURING 'HOLD'.

Q4 RESETS THE INTEGRATOR SHORTING C5 WITH R24. Q4 IS TURNED 'ON' BY A SWITCH IN FREQUENCY RANGE, OR BY THE FRONT PANEL 'RESET' COMMAND (S9A).

5.2.3 - A2 - LOG CONVERSION

THE 916 SWEEP IS LOGARITHMIC TO GIVE MORE NEARLY EQUAL WEIGHTING TO '% OF VALUE' CHANGES IN FREQUENCY OVER THE FREQUENCY RANGE. THE DIODE FUNCTION GENERATOR R26 THRU R34, R60 THRU R66 AND CR11 THRU CR16, AND CR20 CONVERT THE LINEAR SWEEP OUT OF A1 TO A LOG SWEEP OUT OF A2.

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5.2.4 - A2 - FREQUENCY SCALES

THE 'START' FREQUENCY IS THE SECOND INPUT TO A2. IN THE START FREQUENCY RANGE, THE FRONT PANEL R1 SETTING IS THE INPUT. PIN '20' FROM THE START FREQUENCY RANGE COMPARATOR ON BD. #1, IS AT GROUND. Q6 IS 'ON'. THE R1 (F.P.) SETTING IS THE INPUT THRU R35. Q7 AND Q13 ARE ALSO 'ON', EFFECTIVELY SHORTING R42 INPUT TO GROUND.

IN SUCCEEDING FREQUENCY RANGES (IN MULTIDECADE SWEEP), PIN '20' GOES TO -15 VOLTS. Q6 IS 'OFF' BLOCKING THE R1 (F.P.) INPUT. Q7 AND Q13 ARE ALSO 'OFF', CONNECTING R42 AS AN INPUT TO A2 THRU R40, R38, R36. THIS INPUT IS PRECISELY SET FOR 10.0% OF FULL SCALE. THUS, EACH NEW FREQUENCY RANGE STARTS AT 10.0% OF RANGE (MATCHING THE 100% OF PREVIOUS FREQUENCY RANGE).

DURING FREQUENCY RANGE SWITCHING, Q5 OPENS THE INPUT TO A2 SO THAT A2'S OUTPUT DECAYS TO THE START VALUE MORE QUICKLY THAN A1 CAN BE RESET.

A2 OUTPUT DIRECTLY COMMANDS THE DC/FREQUENCY CONVERTER. J1 IS THUS THE DCS1 ALLUDED TO THROUGHOUT THE INSTRUCTION MANUAL.

5.2.5 - A3 - STOP FREQUENCY COMPARATOR

DURING SWEEP, A3 DETERMINES WHEN EACH FREQUENCY RANGE OF THE SWEEP IS COMPLETED. UNTIL THE 'STOP', FREQUENCY RANGE IS REACHED, THE OUTPUT OF A2 IS COMPARED WITH THE SETTING OF R52 (Q8, Q9 & Q10 ARE 'OFF'). THIS IS SET FOR 100% OF FULL SCALE. IN THE 'STOP', FREQUENCY RANGE, Q8, Q9, & Q10 ARE 'ON'. THE COMPARISON IS NOW BETWEEN A2 OUTPUT AND THE SETTING OF STOP FREQUENCY (R2 OF FRONT PANEL) THRU PIN 'B'.

A3 OUTPUT IS NORMALLY AT +.7 VOLTS. IT FLIPS TO -12 VOLTS WHEN DCS1 EXCEEDS THE COMPARATOR INPUT.

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5.2.6 - FREQUENCY RANGE SWITCHING - UL3, UL1

THE U/D COUNTER UL1 IS IN 'PRESET' WHILE S9 (F.P.) IS IN 'RESET'. THE FREQUENCY RANGE COMMANDED BY THE COUNTER OUTPUT (0 TO 5, IN 3 BINARY BITS) IS IDENTICAL TO THE FREQUENCY RANGE COMMANDED BY S1 AS THE PRESET INPUT.

WHEN S9 IS SWITCHED TO SWEEP, UL1 IS REMOVED FROM PRESET. THE COMPLETION OF THE START FREQUENCY RANGE CAUSES A3 TO FIRE THE TWO ONE-SHOTS OF UL3. A3 OUTPUT ALSO PUTS THE SWEEP INTO 'HOLD' (CR7, Q3).

THE SHORT TIME PULSE OUTPUT CAUSES UL1 TO COUNT UP 1 COUNT. THIS MOVES THE FREQUENCY RANGE UP ONE. THE LONGER TIME PULSE OUTPUTS OF UL3 RESET A1, AND REMOVES THE SWEEP INPUT FROM A2 INPUT.

THE FREQUENCY RANGE BEING GREATER THAN THE START FREQUENCY RANGE, THE LOGIC LEVEL AT PIN '21' SWITCHES FROM GROUND TO -15 VOLTS. A2 OUTPUT IS COMMANDED TO 10% OF FREQUENCY SWEEP OR 1.0 VOLT. AS SOON AS THE LONGER ONE-SHOT IS OVER, THE SWEEP WILL REPEAT IN THE NEW FREQUENCY RANGE.

THE ADVANCE OF ONE FREQUENCY RANGE AT A TIME WILL CONTINUE UNTIL THE LOGIC LEVEL AT PIN '1' INDICATES (BY GOING FROM -15 TO GROUND) THAT THE STOP FREQUENCY RANGE HAS BEEN REACHED (SEE BD. #1 FOR STOP AND START FREQUENCY RANGE LOGIC GENERATION).

THEN, Q8, Q9, Q10 & Q11 ARE 'ON'. THE SWEEP IS PUT INTO 'HOLD' WHEN A3 SWITCHES TO -15 VOLTS AS DCS1 EQUALS THE STOP (R2 ON FRONT PANEL) SETTING - THRU TE 'B' & Q8. Q11 PREVENTS THE DUAL ONE-SHOT FROM BEING FIRED. FREQUENCY RANGE DOES NOT ADVANCE.

LOGIC IS PROVIDED IN UL2 AND BY CR21, 22, 23 & R62 TO TURN 'OFF' THE TEST SIGNAL AND TO INDICATE 'END-OF-SWEEP' (DS9 ENERGIZED).

THREE CONDITIONS MUST BE MET TO ENERGIZE 'STOP':

1) FREQUENCY RANGE MUST BE 'STOP' FREQUENCY RANGE - PIN 1 TO CR22.

2) OUTPUT OF A3 MUST INDICATE SWEEP HAS REACHED STOP SETTING - PIN 15 TO UL2-D TO CR23.

3) SWEEP IS NOT IN 'RESET' - PIN '2' THRU UL2B TO CR21.

THE 3 DIODES, CR21, 22, 23, FORM AN 'AND' GATE ON CONDITIONS 1, 2, & 3. A (-1 AMP) BRINGS OUT TO PIN 'R' THE RESET, STOP COMMAND. A SECOND (-1 AMP) BRINGS THE PLUS 'RESET', SWEEP STOP COMMAND TO PIN 'K'.

5.2.7 - FREQUENCY RANGE SWITCHING INTERLOCK

J2E IS CONNECTED TO END-OF-CYCLE (J19-11). IT INHIBITS FREQUENCY RANGE SWITCHING UNTIL THE MODE CORRESPONDS TO THE EOC SIGNAL. THUS FREQUENCY RANGE SWITCHES AS 'RESET' STARTS, AND EVERY CYCLE OF ANALYSIS IS A GOOD ONE.

SWITCHING FREQUENCY RANGE FROM 1.0 TO 10. IS INTERLOCKED ON THE 'X5' INTEGRATE BOARD, TO PREVENT A LOCKUP OF THE DC/FREQUENCY CONVERTER. PIN '22' IS GROUNDED WHENEVER THE UNDESIRABLE FREQUENCY RANGE SWITCH CONDITION OCCURS. A3 FIRES THE ONE-SHOT AS SOON AS PIN '22' IS RETURNED TO -15 VOLT. AT MOST, THIS CONDITION DELAYS FREQUENCY RANGE SWITCHING BY 1/2 CYCLE OF THE TEST FREQUENCY. THE SWEEP IS ON 'HOLD', SO NO DATA IS LOST.

J2D IS CONNECTED TO J2-2, SO THAT FREQUENCY RANGE SWITCH COMMAND CANNOT BE GENERATED WHEN IN 'RESET' (FREQUENCY-BY-FREQUENCY TESTING) AND INADVERTENTLY THE START FREQUENCY EXCEEDS THE STOP FREQUENCY SETTING.

5.2.8 - TEST POINTS & ADJUSTMENTS

J2 - FREQUENCY RANGE SWITCH COMPARATOR OUTPUT NORMALLY -12 TO -15 VOLTS. WHEN FREQUENCY EXCEEDS STOP FREQUENCY, GOES TO +.7 VOLTS.

J1 - DCS1 - DC VOLTAGE LINEAR WITH FREQUENCY +10.0 VOLTS FULL SCALE. LIN. FREQ.

R20 - 'HOLD' ADJUST FOR A1. SET FOR ZERO DRIFT IN FREQUENCY DURING HOLD.

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5.2.8 - TEST POINTS & ADJUSTMENTS (CONT'D)

R42 - 10% OF FULL SCALE ADJUST FOR START OF FREQUENCY RANGE DURING SWEEP (SEE SEC. 6.9.2 FOR ADJUSTMENT).

R52 - 100% OF FULL SCALE ADJUST FOR STOP OF FREQUENCY RANGE DURING SWEEP (SEE SEC. 6.9.2 FOR ADJUSTMENT).

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5.3 & 4 - INPUT AMPLIFIER - BOARDS #3 & #4

REFERENCE: DRAWING NO. C103110
SEC. 4.5.1 - THEORY OF INPUT AMPLIFIER
SEC. 4.8 - AUTOMATIC GAIN CONTROL

5.3 & 4.1 - FUNCTION

THE INPUT AMPLIFIER BOARD AMPLIFIES THE INPUT SIGNAL (FROM ITS RESPECTIVE PREAMPLIFIER) BY THE GAIN COMMANDED BY THE AUTOMATIC GAIN CONTROL (BOARD #5).

GAIN IS SET IN BINARY STEPS FROM X1, X2- - - - , X1024 VOLTS/VOLT.

HIGH PASS ACTION TO FURTHER INPROVE LOW FREQUENCY NOISE REJECTION IS INCLUDED. THE BREAK FREQUENCY IS INCREASED A DECADE AT A TIME TO CORRESPOND TO A FIXED PERCENTAGE OF THE OPERATING FREQUENCY RANGE.

A DC OUTPUT PROPORTIONAL TO THE GAIN SETTING IS GENERATED.

LOGIC LEVEL TO INDICATE THE HIGHEST GAIN SETTING IS GENERATED.

5.3 & 4.2 - AMPLIFIERS

AMP. 1 - 318

AMP 1 HAS GAIN OF 1/1 (Q1 & Q2 OFF), 2/1 (Q1 ON, Q2 OFF), 4/1 (Q2 ON, Q1 OFF), 5/1 (Q1 & Q2 ON).

AMP 2 - 318

GAIN OF 1/1, (Q3 OFF & Q4 OFF).
GAIN OF 8/5, (Q3 ON & Q4 OFF).
THIS SETTING IS USED ONLY WHEN Q1 AND Q2 ARE 'ON' AS DETERMINED BY CR1, CR2, R5 'AND' GATE. THUS, NET GAIN OF A1 A2 IS 8/1.

GAIN OF 16/1 (Q4 ON, Q3 OFF).
CONDITION Q4 'ON', Q3 'ON' IS NOT USED.
R10, C7 EQUALIZES PHASE RESPONSE AT 16/1 GAIN FOR HIGH FREQUENCY RANGE.

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916 XH

AMP 3 - 318

GAIN OF 1/1 (Q5 OFF).
GAIN OF 16/1 (Q5 ON).
R25 C19 EQUALIZES PHASE SHIFT AT 16/1 GAIN.

GAIN IS COMMANDED BY FOUR LINES CORRESPONDING TO:

PIN A - X1, X2;
PIN B - X1, X4;
PIN 4 - X1, X16;
PIN 3 - X1, X256.

THESE LOGIC LEVELS PASS THRU THE '+1' BUFFERS OF UL1 TO DRIVE AS FOLLOWS:

PIN A - TO - Q1
PIN B - TO - Q2
PIN 4 - TO - Q5
PIN 3 - TO - Q4 & Q5

CR1, CR2, R5 PROVIDE THE 'AND' GATE TO Q3 WHEN 'X2' & 'X4' ARE COMMANDED TO GIVE THE GAIN OF 'X8'.

CR5, CR6, R38 PROVIDE THE 'OR' GATE TO TURN Q5 ON TO GIVE 'X16' ON A3 FOR BOTH PIN 3 & PIN 4. PIN 3 ALSO TURNS Q4 'ON' FOR X256.

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THE NET RESULT IS AS FOLLOWS:

+1 = GROUND

0 = -15

GAIN	PIN				FET				
VOLTS/ VOLT	A	B	4	3	Q1	Q2	Q3	Q4	Q5
X1	0	0	0	0	OFF	OFF	OFF	OFF	OFF
X2	1	0	0	0	ON	OFF	OFF	OFF	OFF
X4	0	1	0	0	OFF	ON	OFF	OFF	OFF
X8	1	1	0	0	ON	ON	ON	OFF	OFF
X16	0	0	1	0	OFF	OFF	OFF	OFF	ON
X32	1	0	1	0	ON	OFF	OFF	ON	OFF
X64	0	1	1	0	OFF	ON	OFF	ON	OFF
X128	1	1	1	0	ON	ON	ON	ON	OFF
X256	0	0	0	1	OFF	OFF	OFF	ON	ON
X512	1	0	0	1	ON	OFF	OFF	ON	ON
X1024	0	1	0	1	OFF	ON	OFF	ON	ON

THE GAIN IS THUS CONTROLLED BY A BINARY COMMAND IN 11 STEPS FROM X1 THRU X1024 VOLTS/VOLT (IN X2 STEPS).

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5.3 & 4.3 - A4 - HIGH PASS FILTER

A4 IS CONNECTED AS AN INTEGRATOR. IT CLOSES THE LOOP AROUND A3 OUTPUT TO A2 INPUT IN SUCH A SENSE AS TO KEEP THE DC CONTENT AT A3 OUTPUT NEAR ZERO. THEN A3 OUTPUT OVER A1 OUTPUT EQUALS -

$$\frac{\text{A3 OUT}}{\text{A1 OUT}} = \frac{\text{GAIN} \quad \frac{FR}{K} \cdot \frac{J\omega}{\omega_O}}{1 + \frac{FR}{K} \cdot \frac{J\omega}{\omega_O}} \qquad (5.3\text{-}1)$$

K = LOOP GAIN (APPROXIMATELY 312.5)

WHERE ω_O = FILTER BREAK FREQUENCY (IN RAD./SEC.).

FR - FREQUENCY RANGE

THE BREAK FREQUENCY IS MOVED IN DECADES BY THE CONDENSERS C15, C13 AND C14 AND THE INPUT RESISTORS R1, R22, AS FOLLOWS:

F.R.	Q8	Q9	Q14
HZ	C13 IN // WITH C14 WHEN 'ON'	C15 IN // WITH C14 WHEN 'ON'	R22 IN // WITH R21 WHEN 'ON'
100K	OFF	OFF	ON
10K	OFF	OFF	OFF
1K	OFF	ON	ON
100	OFF	ON	OFF
10	ON	ON	ON
1	ON	ON	OFF

WHEN A3 HAS A GAIN OF 'X16' (Q5 ON) Q6 GOES 'ON' AND R27 IS ADDED TO ATTENUATE THE LOOP GAIN BY 1/16 AND KEEP THE NET LOOP GAIN CONSTANT.

THE CONDENSERS ARE SELECTED AND THE LOOP GAIN SET TO MATCH THE PHASE SHIFT AT THE LOW END OF FREQUENCY RANGE FOR ALL FREQUENCY RANGES AND GAIN SETTINGS.

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5.3 & 4.4 - A5 - DB VS. GAIN - 0.1 VOLT/DB -

A5 OUTPUT IS LINEAR VS. GAIN, OR IS THE DB PROPORTIONAL TO GAIN SETTING. A GAIN OF X1, GIVES ZERO OUTPUT. EACH DOUBLING OF THE GAIN ADDS +0.6 VOLTS TO THE OUTPUT.

GAIN	FET(S)	OUTPUT-VOLTS
X2	Q10	+.60
X4	Q11	+1.20
X8	Q10, Q11	+1.80
X16	Q12	+2.40
X32	Q10, Q12	+3.00
X64	Q11, Q12	+3.60
X128	Q10, Q11, Q12	+4.20
X256	Q13	+4.80
X512	Q10, Q13	+5.40
X1024	Q11, Q13	+6.00

5.3 & 4.5 - HIGH COUNT

Q7, CR3, CR4 - $\overline{\text{HIGH}}$ $\overline{\text{COUNT}}$ LOGIC

THE HIGHEST GAIN COMMAND ALLOWABLE IS 'X1024'. CR3, CR4, R37 FORM THE 'AND' GATE TO RESPOND TO 'X4·X256'. WHEN BOTH LINES ARE AT GROUND (ON), Q7 GOES OFF, AND THE OUTPUT AT PIN 'C' IS NEAR -15 VOLTS. (USED IN AUTOMATIC GAIN CONTROL TO PREVENT MOVEMENT OF COUNTER TO A HIGHER COUNT OR HIGHER GAIN).

5.3 & 4.6 - ADJUSTMENTS & TEST POINTS

R18 SETS A3 OUTPUT NEAR ZERO DC. ADJUST FOR MINIMUM DC LEVEL AT TWO ADJACENT FREQUENCY RANGES.

R60 SETS SPAN OF DB CIRCUIT AT 0.6 VOLTS/6DB. SET AT HIGH GAIN AND USING A DVM. FOR EXAMPLE, DEPRESS FRONT PANEL SWITCH FOR PRESET GAIN (S10). A5 OUTPUT AT J2 SHOULD BE +4.80 VOLTS

J0 - GROUND
J1 - OUTPUT OF INPUT AMPLIFIER
J2 - DB GAIN (.6 VOLT/6DB) OUTPUT

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5. (3 & 4) .7 - HIGH FREQUENCY COMPENSATION - SPECIAL TO 916XH

REFERENCE: DRAWING #C103110-5

THE INPUT AMPLIFIERS OF THE 916XH ARE COMPENSATED FOR PHASE RESPONSE AT GAINS HIGHER THAN 'X1'. THE COMPENSATION MAKES THE PHASE RESPONSE AT A GAIN OF X2, X4,-----X1024 IDENTICAL TO THAT AT X1 WHEN OPERATING AT 100 KHZ.

THE VALUES GIVEN ARE TYPICAL. THE 'C' VALUES MAY BE SELECTED TO OPTIMIZE THE PHASE.

THE COMPONENTS USED ARE RELATED TO GAIN AS FOLLOWS:

X2 ('A' AT GROUND) - C35

X4 ('5' AT GROUND) - C36

X8 ('A & 5' AT GROUND) - R63, C37

X16 ('4' AT GROUND) - R25, C19, C38 (ADJ)

X256 ('3' AT GROUND) - R10, C7

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916 XH

5.5 AUTOMATIC GAIN CONTROL BOARD #5

REFERENCE: DRAWING NO. C103116 &
BLOCK DIAGRAM NO. 4.8-1
SECTION 4.8 FOR THEORY OF OPERATION

NOTE: THE NUMBERS IN PARENTHESES APPLY TO CHANNEL #2. THE EXPLANATION IS OF CHANNEL #1.

5.5.1 - PURPOSE

THE AUTOMATIC GAIN CONTROL SYSTEM SETS THE GAIN OF THE INPUT AMPLIFIER TO GIVE THE OPTIMUM ANALYSIS. THERE ARE THREE CAUSES FOR CHANGING THE GAIN.

(1) THE SIGNAL PLUS NOISE MAY EXCEED THE DYNAMIC RANGE OF THE MULTIPLIER INPUT OF ±10 VOLTS = 'S+N' O.L.

(2) THE SIGNAL AMPLITUDE MAY EXCEED THE RANGE SET IN THE COMPUTING CIRCUITS. THIS IS DETERMINED BY THE COMPARATORS ON THE AMPLITUDE RATIO BOARD #12, AND IS EQUIVALENT TO SIGNAL OF ±5 VOLTS AT INPUT TO MULTIPLIER - SIGNAL OVERLOAD.

(3) THE SIGNAL AMPLITUDE MAY BE LESS THAN THE MINIMUM LEVEL FOR ACCURATE SIGNAL ANALYSIS. THIS IS DETERMINED FROM SIGNAL AMPLITUDE BY COMPARATORS ON THE AMPLITUDE RATIO BOARD. IT IS EQUIVALENT TO ±2 VOLTS OF SIGNAL AT THE INPUT TO THE MULTIPLIERS. - SIGNAL UNDERLOAD.

THE RESPONSE OF THE AUTOMATIC GAIN CONTROL TO EACH OF THESE CONDITIONS IS GIVEN BELOW:

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5.5.2 - 'S+N' OVERLOAD - SIGNAL PLUS NOISE OVERLOAD

REFERENCE: DRAWING NO. 103116

THE INPUT AMPLIFIER DRIVES PIN 'Z' (20). Q3 (Q1) IS NORMALLY 'OFF' AND Q4 (Q2) IS BIASED 'ON'. WHEN THE INPUT EXCEEDS +10 VOLTS, Q4 IS TURNED 'OFF' AND THE ONE-SHOT IS TRIGGERED. WHEN THE INPUT IS MORE NEGATIVE THAN -10 VOLTS, Q3 (Q1) IS TURNED 'ON' AND THE ONE-SHOT IS TRIGGERED. THE PULSE THRU CR6 (CR2) CAUSES UL4 (UL5) TO COUNT DOWN 1 - OR REDUCE THE GAIN OF ITS INPUT AMPLIFIER BY 1/2.

AT THE SAME TIME, FET 'Q6' (Q5) IS TURNED 'ON', SHORTING THE INPUT SIGNAL. THIS RESTORES THE COMPARATOR TRANSISTORS Q3, Q4, (Q1, Q2) TO THEIR NORMAL STATE. IF THE OVERLOAD IS REMOVED BY THE END OF THE ONE-SHOT PERIOD, NOTHING MORE OCCURS. IT THERE WERE A MASSIVE OVERLOAD, THE COMPARATOR WILL AGAIN DETECT IT, TRIGGER THE ONE-SHOT AND REDUCE THE GAIN BY 1/2. THIS CONTINUES UNTIL NO 'S+N' OVERLOAD EXISTS.

NOTE HOW RAPID THIS SEQUENCE IS.

THE LOGIC INTERLOCKS TO PREVENT THIS RESPONSE FROM GOING TOO FAR ARE:

(1) WHEN THE DOWN COUNT ACTION REACHES 0000 ON THE U/D COUNTER, PIN 7 OF (UL5) UL4 GOES TO -15. (UL2A) UL1B BLOCKS THE OVERLOAD PULSE AND LEAVES THE COUNTER COMMANDING THE MINIMUM GAIN.

(2) THE 'S+N' OVERLOAD PULSE RESETS THE ANALYZER (SEC. 5.16 - TIMING BOARD) TO ABORT THE ANALYSIS CYCLE DURING WHICH THE 'S+N' OVERLOAD OCCURRED.

IF THE ANALYZER COMPLETES THE ANALYSIS PORTION OF THE ANALYSIS CYCLE, AND GOES INTO THE COMPUTE PORTION, THERE IS NO NEED TO RESET THE ANALYZER. THE RESULTS CAN BE READ OUT.

UL6 IS INHIBITED BY DRIVING ITS PINS 3 AND 13 TO -15 VOLTS. R41, C23 SLOW UP THE RELEASE FROM THE INHIBIT CONDITION TO PREVENT TRANSIENTS FOLLOWING GAIN CHANGE AT THE START OF 'RESET' FROM CAUSING A 'S+N' RESPONSE.

THE SWEEP IS DRIVEN TO 'HOLD' AS LONG AS 'S+N' OVERLOAD PERSISTS.

5.5.3 - SIGNAL UNDERLOAD

THE PRESENCE OF A SIGNAL UNDERLOAD IS NOTED DURING THE 'HOLD' PORTION OF THE ANALYSIS CYCLE. THE START OF RESET GENERATES A PULSE (SEE 'X5' INTEGRATE BOARD). UL1D (UL2C) RESPONDS TO (SIGNAL UNDERLOAD·RESET). THIS TRIGGERS UL3. ITS OUTPUT PULSE SETS THE U/D COUNTER UL4 (UL5) IN THE COUNT 'UP' MODE. THE COUNTER GOES UP 1 COUNT. GAIN IS INCREASED 2/1.

THERE IS NO PAUSE IN THE ANALYZER CYCLE OF OPERATION. THE NORMAL COURSE OF SIGNAL LEVEL VARIATION, THE UNDERLOAD IS NOT SEVERE ENOUGH TO CAUSE SIGNIFICANT ERRORS. THE UNDERLOAD IS REMOVED BY THE GAIN INCREASE. THE RESET PERIOD PROVIDES TIME FOR THE INPUT AMPLIFIER TO SETTLE OUT FROM THE GAIN CHANGE.

LOGIC PREVENTS THE COUNT FROM EXCEEDING 1010. THE HIGH COUNT LOGIC LEVEL FROM THE INPUT AMPLIFIER BLOCKS THE COUNT UP PULSE AT UL1A (UL2B). THE CONTINUED PRESENCE OF AN UNDERLOAD LIGHT ENERGIZED, INDICATES LESS THAN 2.0 MV OF SIGNAL IN THE RETURN SIGNAL.

5.5.4 - SIGNAL OVERLOAD

THE SIGNAL OVERLOAD IS DETECTED DURING THE 'HOLD' PORTION OF THE ANALYSIS CYCLE. UL1C (UL2D) PASSES THE RESET PULSE FROM 'X5' INTEGRATE BOARD) TO DRIVE THE RESPECTIVE COUNTER DOWN 1 COUNT AND REDUCE THE GAIN BY 1/2.

AS BEFORE, IF THE COUNTER IS AT 0000, THE COUNT DOWN IS BLOCKED (GAIN AT X1, AND MORE THAN ±5 VOLT OF SIGNAL CONTENT AT MULTIPLIER INPUT) (±10 VOLT AT ANALYZER INPUT). RESET PERIOD ALLOWS FOR SETTLING OF INPUT AMPLIFIER.

5.5.5 - CALIBRATION - NONE

- TEST POINTS - NONE

- ADJUSTMENTS - NONE

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5.6 - WAVEFORM SELECT

REFERENCE: DRAWING #C103634

5.6.1 - FUNCTIONS

BOARD #6 PROVIDES THE SELECTOR CIRCUITS SO THAT THE WAVEFORM COMMANDS FROM THE FRONT PANEL, CAUSE 'SIN', 'TRIANGLE' OR 'SQUARE' WAVE TO BECOME THE DRIVER OF THE 'OUTPUT' CIRCUITS.

5.6.2 - OPERATION

AMP 4 IS THE ADJUSTABLE TRIANGLE PHASE SHIFT. 'C10' IS THE PHASE ADJUSTMENT TO MAKE 'SIN' EXACTLY 90° OUT-OF-PHASE WITH 'COS' TO 50 KHZ. THE PROCEDURE IS GIVEN IN SEC. 6.11-H.

PINS 'K' AND 'M' CONTROL THE SELECTION OF PIN 'B' (SIN), PIN 'C' (SQUARE), PIN 'V' (TRIANGLE) AS THE INPUT TO AMP 1 THUS AS THE TEST SIGNAL OUTPUT WAVESHAPE.

IF 'K' AND 'M' ARE NOT GROUNDED, Q2 IS DRIVEN 'ON' (BY R20, R8), Q1 IS 'ON' (Q2 AND Q3 ARE 'OFF'), AND THE 'SIN' OF PIN 'B' DRIVES AMP 1.

IF 'K' IS GROUNDED, Q4 IS 'OFF' (R9 DRIVES IT OFF), Q2 IS 'ON'. THE SQUARE WAVE FROM PIN 'C' BECOMES THE INPUT TO AMP 1.

IF 'M' IS GROUNDED, Q4 IS 'OFF', Q3 IS 'ON'. THE TRIANGLE WAVE AT PIN 'Y' BECOMES THE INPUT TO AMP 1.

NOTE THE FRONT PANEL SWITCHES SO NOT PERMIT PINS 'K AND M' TO BE GROUNDED SIMULTANEOUSLY.

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5.7 & 8 - DUAL MULTIPLIER - INTEGRATOR

REFERENCE: DRAWING #C102973
SECTION 4.5.2 FOR THEORY

5.7 & 8.1 - FUNCTION

1) MULTIPLY THE OUTPUT OF THE INPUT AMPLIFIER BY 10· SINωt AND 10· COSωt.

2) ATTENUATE THE PRODUCTS INVERSELY AS FREQUENCY.

3) INTEGRATE EACH PRODUCT TO FORM THE IN-PHASE AND QUADRATURE COMPONENT ON THE FUNDAMENTAL OF THE RETURN SIGNAL, SCALED FOR ALL FREQUENCY RANGES, AND 'X5' OPERATION.

5.7 & 8.2 - MULTIPLICATION

TRANSCONDUCTANCE MULTIPLIERS ARE USED IN THE 916 BECAUSE OF THEIR ACCURACY, BANDWIDTH AND SIMPLICITY.

THE IN-PHASE CHANNEL IS DESCRIBED WITH THE EQUIVALENT QUADRATURE CHANNEL IN PARENTHESES.

A3 (A1) IS THE IN-PHASE (QUADRATURE) MULTIPLIER. THE INPUT SIGNAL FROM THE INPUT AMPLIFIER IS ON PIN '5'. THE REFERENCE 10· SINωt (10· COSωt) IS ON PIN 'M' (PIN 'Z').

ZERO DC OUTPUT IS SET BY R36 (R12). FOR GREATER SENSITIVITY, STABILITY, AND EASE OF SETTING, THESE POTS ARE EXCITED FROM A STABLE 6 VOLT REFERENCE. ALL OF THE ABOVE ADJUSTMENTS ARE DESCRIBED IN DETAIL IN SECTION 6.4 OF THE MANUAL.

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5.7 & 8.3 - ATTENUATOR

Q1 (Q2) GIVES THE ATTENUATION ACTION AS COMMANDED BY THE ATTENUATOR CIRCUIT ON THE 7 KHZ BOARD.

WHEN Q1 (Q2) IS 'ON', IT NEARLY SHORTS R13 (R37) TO GROUND AND BLOCKS SIGNAL FROM GOING TO THE INTEGRATOR. WHEN Q1 (Q2) IS 'OFF', ALL OF THE SIGNAL DRIVES INTO THE INTEGRATOR. THE ATTENUATOR CIRCUIT PORTIONS THE 'ON' TIME VS. 'OFF' TIME AT 7 KHZ TO OBTAIN THE DESIRED ATTENUATION.

IN THE TWO HIGH FREQUENCY RANGES, Q1 (Q2) IS KEPT 'OFF' AS INTEGRATE TIME IS FIXED (AND IS NOT INVERSELY PROPORTIONAL TO FREQUENCY).

5.7 & 8.4 - INTEGRATION

A2 (A4) IS THE INTEGRATOR. IT HAS THREE MODES OF OPERATION:

1) IN 'RESET', PIN '2' IS AT GROUND, AND Q3 (Q10) IS 'ON' SHORTING THE FEEDBACK CONDENSER AND REDUCING THE AMPLIFIER OUTPUT TO NEAR ZERO.

   Q11 (Q12) IS KEPT 'OFF' - PIN 'F' AT -15, DURING MOST OF THE 'RESET' PORTION OF THE ANALYSIS CYCLE TO PREVENT ANY LEVEL BEING FORCED ON THE INTEGRATOR OUTPUT (IN 'RESET', GAIN IS SMALL BUT NOT ZERO).

2) IN 'OPERATE' (INTEGRATE), Q11 (Q12) IS 'ON' (PIN 'F' AT GROUND), AND Q3 (Q10) IS 'OFF' (PIN '2' AT -15). THE INTEGRATION CONTINUES FOR A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY.

3) IN 'HOLD', Q11 (Q12) IS 'OFF' AND Q3 (Q10) IS 'OFF'. THE INTEGRATE CONDENSER AND AMPLIFIER 'HOLD' THEIR LAST D.C. LEVEL (RESULT OF INTEGRATION).

3) SCALING OF THE INTEGRATION CONSTANT FOR THE DIFFERENT FREQUENCY RANGES, AND FOR 'X5' INTEGRATE IS ACCOMPLISHED BY TWO STRATAGEMS: IN THE TWO LOWEST FREQUENCY RANGES, AND IN ALL SIX FREQUENCY RANGES WHEN IN 'X5' INTEGRATE, PIN '4' IS AT GROUND; INCREASING THE INTEGRATE CONSTANT BY 5/1 (1.25 MF TO 6.25 MF). IN THE TWO LOWEST FREQUENCY RANGES, THE OPERATE-HOLD FUNCTION IS MODULATED IN TIME (Q11, Q12). FROM .005 TO .1 HZ, Q11 (Q12) IS 'ON' FOR 10% OF THE TIME, AND 'OFF' (IN HOLD) 90% OF THE TIME WHEN NOT IN 'X5' INTEGRATE ('X5'). THIS GIVES AN APPARENT INTEGRATE CONSTANT INCREASE OF 10/1

REMEMBERING THAT THE INTEGRATE TIME IS INCREASED 2/1 IN THE LOWEST TWO FREQUENCY RANGES IN 'X5'; THE 'ON' TIME IS REDUCED TO 5% OF TOTAL OPERATE TIME IN THE .005 - .1 HZ FREQUENCY RANGE, AND TO 1/2 THE TIME FROM 0.1 HZ THRU 1.0 HZ. THIS DOUBLES THE EQUIVALENT INTEGRATE CONSTANT, WITH 'X5' IN.

5.7 & 8.5 - TEST POINTS & ADJUSTMENTS

(SEE SEC. 7 - FAST CHECKOUT & ADJUSTMENT)

J1	-	OUTPUT OF MULTIPLIER-A1
J2	-	OUTPUT OF INTEGRATOR-A2 - QUADRATURE
J3	-	OUTPUT OF INTEGRATOR-A4 - IN-PHASE
J4	-	OUTPUT OF MULTIPLIER-A3
R12	-	ZERO ADJUST MULTIPLIER-A1
R19	-	ZERO DRIFT ADJUST - INTEGRATOR-A2
R36	-	ZERO ADJUSTMENT - MULTIPLIER-A3
R52	-	ZERO DRIFT ADJUST - INTEGRATOR-A4

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5.9 - SIN-COS-LOG FREQUENCY

REFERENCE: DRAWING NO. C104473 - SHEETS 1 & 2

5.9.1 - FUNCTIONS

THIS BOARD DOES THE FOLLOWING:

1) SHAPE THE TRIANGLE WAVEFORM FROM DC/FREQUENCY BOARD INTO A SINE WAVE OF LOW DISTORTION.

2) SHAPE TRIANGULAR WAVEFORM INTO COSINE WAVE.

3) FORM DC SIGNAL PROPORTIONAL TO LOG FREQUENCY FROM DCS1 AND FREQUENCY RANGE DIGITAL COMMANDS.

5.9.2 - SINE WAVE

THE TRIANGLE FROM DC/FREQUENCY BOARD DRIVES THE 14 BREAK POINT DIODE FUNCTION GENERATOR (CR18 - CR33; R52 - R81) WHICH REDUCES GAIN WITH INPUT AMPLITUDE IN AN OPTIMUM MANNER SO THAT A5 OUTPUT IS 10 SIN ωt. DISTORTION IS WELL UNDER 1% TOTAL RMS (FACTORY ADJUSTED TO UNDER 1/2% TO 1000 HZ).

R82 PRECISELY SETS THE ZERO DC OUTPUT.

R85 SPANS THE OUTPUT.

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5.9.3 - LOG FREQUENCY

REFERENCE: DRAWING NO. C104473 - SHEET 2

A4, Q4 PERFORM THE NONLINEAR OPERATION OF CONVERTING THE DC VOLTAGE LINEARLY PROPORTIONAL TO FREQUENCY (WITHIN EACH FREQUENCY RANGE) TO A DC VOLTAGE LOGARITHMICALLY PROPORTIONAL TO FREQUENCY.

Q4, IN THE FEEDBACK OF A4, IS A TEMPERATURE STABILIZED TRANSISTOR. THE OUTPUT OF A4 CHANGES 79 OR 80 MV PER DECADE CHANGE OF INPUT.

A4 OUTPUT IS SCALED BY A3 TO 2.00 VOLT/DECADE. (25 VOLTS/ VOLT GAIN) WITH R80 AS THE PRECISE ADJUSTMENT.

R77 BIASES OUT MOST OF A4, Q4 DC OFFSET (ABOUT 400 MV). R72 PRECISELY ADJUSTS FOR THE REMAINDER.

Q1, Q2, Q3 BRING IN THE OFFSETS TO MAKE THE LOG FREQUENCY OUTPUT CONTINUOUS FROM -4.00 VOLTS AT 0.1 HZ, TO +8.00 VOLTS AT 100 KHZ. R74, R75, R76, R78 ARE SELECTED FOR A PRECISE FIT TO THE 2.00 AND 4.00 VOLT OFFSETS.

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5.10 - DC/FREQUENCY

REFERENCE: DRAWING NO. C104470
& SEC. 4.4.2 - THEORY OF OPERATION

5.10.1 - FUNCTION

THE DC/FREQUENCY BOARD GENERATES A FIXED AMPLITUDE TRIANGLE WAVEFORM AT THE DESIRED FREQUENCY OF OPERATION. IT RESPONDS TO THE FREQUENCY RANGE COMMAND LINES FROM THE EXTENDED SWEEP BOARD #2, AND TO THE FREQUENCY COMMAND FROM THE SAME BOARD.

A SQUARE WAVE IS ALSO GENERATED THAT CHANGES STATE AT THE PLUS AND MINUS PEAKS OF THE TRIANGLE.

5.10.2 - SCALING & INVERTING AMPLIFIERS A1A, A1B

THE DCS1 INPUT ON PIN 'W' IS SCALED BY A1A TO CALIBRATE AGAINST THE INTEGRATOR (A2) CONDENSERS.

Q7 IS 'ON' IN FR (1 & 2) MAKING R50 THE SCALING POTENTIOMETER.

Q8 IS 'ON' IN FR (3 & 4) MAKING R51 THE SCALING POTENTIOMETER.

Q9 IS 'ON' IN FR (5 & 6) MAKING R52 THE SCALING POTENTIOMETER.

A1B PROVIDES A (-1) OF A1A OUTPUT. A1A OUTPUT IS ALWAYS MINUS, AND A1B IS ALWAYS PLUS.

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5.10.3 - INTEGRATOR A2 - FREQUENCY RANGE SELECTION

AMP 2 INTEGRATES ITS INPUT TO FORM THE TRIANGLE OUTPUT. WHEN THE INPUT IS PLUS, IT INTEGRATES IN A NEGATIVE GOING SENSE UNTIL IT REACHES -10 VOLTS. THE INPUT IS SWITCHED TO MINUS, AND A2 INTEGRATES IN A POSITIVE GOING SENSE UNTIL IT REACHES +10 VOLTS. THE PROCESS REPEATS. AS THE INPUT IS A SCALED DCS1 FROM A1A AND A1B, FREQUENCY IS LINEARLY PROPORTIONAL TO DCS1.

A3, UL1 PERFORM THE SWITCHING AT ±10 VOLTS. A1A AND A1B PROVIDE THE MINUS AND PLUS INPUTS.

FOUR LINES DETERMINE THE FREQUENCY RANGE. PIN 'X' COMMANDS 'ALT' F.R. IT SELECTS THE INPUT RESISTORS TO A2. WHEN 'ON' (AT GROUND) WHICH CORRESPONDS TO THE HIGHER OF THE TWO RANGES, Q4 AND Q5 ARE 'ON', PARALLELING R 7 & 8 WITH R9, AND R5 WITH R6. THE VALUES ARE SELECTED TO DECREASE THE RESISTANCE BY 10/1 AND THUS INCREASE THE FREQUENCY BY 10/1.

PIN 'E' COMMANDS FREQUENCY RANGES (1 + 2). THIS LOGIC LEVEL IS FROM THE 'X5' INTEGRATE BOARD #1 WHERE IT IS COMPUTED AS $\overline{3+4+5+6}$. PIN 'E' TURNS ON Q7 AND Q1. THUS A2 HAS C6, C4, C5 AND C7 IN PARALLEL. THIS GIVES THE LOWEST TWO FREQUENCY RANGES. AS HIGHER RANGES ARE COMMANDED, CONDENSERS ARE DISCONNECTED FROM THE FEEDBACK PATH (RATHER THAN ONE BEING DISCONNECTED AND ONE BEING ADDED).

PIN 'D' COMMANDS FREQUENCY RANGES (3 + 4) (FROM EXTENDED SWEEP BOARD #2). IT DROPS C4 FROM THE FEEDBACK, AND LEAVES C7, C5 AND C6 BY TURNING Q2 ON.

PIN 'C' COMMANDS FREQUENCY RANGES (5 + 6) (FROM EXTENDED SWEEP BOARD #2). IT DROPS C5 AND LEAVES C7 AND C6 IN THE FEEDBACK OF A2.

IN THIS WAY THE SIX FREQUENCY RANGES ARE SET UP.

PIN 'F' PUT AT GROUND, TURNS Q10 'ON' AND RESETS THE TRIANGLE WAVE. IF, AT A PLUS POTENTIAL, IT IS BROUGHT IMMEDIATELY TO +.7 VOLTS. IF, AT A MINUS POTENTIAL, IT COMPLETES THAT PORTION OF ITS CYCLE AND SLIDES INTO THE +.7 VOLT LEVEL.

R4 BALANCES THE PLUS AND MINUS SLOPES OF THE TRIANGLE.

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5.10.4 - COMPARATOR - A3

A3 IS A COMPARATOR THAT TURNS ON UL1.

THE OUTPUT DRIVES THE SWITCH CR7, 8, 9, 10. CR11 IS A 6 VOLT ZENER DIODE. THE DIODE SWITCH CONDUCTS CURRENT THROUGH THE ZENER DIODE IN THE SAME SENSE FOR PLUS INPUT (CR9, CR11, CR8) AS FOR MINUS INPUT (-CR10, -CR11, -CR7). THE RESULT IS A 7 VOLT SQUARE WAVE AT THE COMMON OF R32, R31, CR9, CR10. THE ±7 VOLTS IS THE COMPARATOR FEEDBACK.

WHEN A2 OUTPUT REACHES +10 VOLTS, IT OVERCOMES THE MINUS INPUT FROM THE DIODE SWITCH AND A3 FLIPS TO A PLUS OUTPUT. WHEN A2 OUTPUT REACHES -10 VOLTS, IT OVERCOMES THE PLUS INPUT FROM THE DIODE SWITCH AND A3 FLIPS TO A MINUS OUTPUT.

CR5, 6 FORM A TEMPERATURE STABILIZING FEEDBACK TO A3 TO OVERCOME THE TEMPERATURE DRIFT IN CR7, 8, 9, 10.

R14 SCALES THE TRIANGLE AMPLITUDE VS. THE SWITCH OUTPUT.

R33, C13 SPEED UP THE SQUARE WAVE RISE TIME TO THE FEEDBACK AT HIGH FREQUENCY. IT HELPS INSURE NOISE FREE SWITCHING ACTION.

R15, C11, C12 OVERCOME A3 SWITCHING TIME EFFECTS ON FREQUENCY LINEARITY AT HIGH FREQUENCY.

R20 BALANCES +10 AND -10 VOLT TRIANGLE EXCURSION.

5.10.5 - TEST POINTS & ADJUSTMENTS

J0	-	GROUND
J1	-	TRIANGLE WAVESHAPE
J2	-	SQUARE WAVE
R20	-	ADJUST TRIANGLE TO ZERO DC LEVEL
R50	-	SPAN OF FR (1 + 2)
R51	-	SPAN OF FR (3 + 4)
R52	-	SPAN OF FR (5 + 6)
R28	-	ADJUST TRIANGLE TO ZERO DC LEVEL IN RANGE 6 (100 KHZ)

THESE ADJUSTMENTS NEED BE MADE ONLY ON OVERALL INSTRUMENT CALIBRATION. FOLLOW INSTRUCTIONS OF SECTION 6.3.

5.10.6 - COSINE GENERATION

A TRIANGLE WAVEFORM OF ±10 VOLTS IS GENERATED THAT IS 90° PHASE SHIFTED FROM THE SIN TRIANGLE. THE SAME INPUTS (FROM A1A AND A1B) ARE USED TO GENERATE BOTH TRIANGLES. THE SIN TRIANGLE SWITCHES THE COMPARATOR AT THE ±10 VOLT POINT AND SWITCHES THE COSINE COMPARATOR EACH TIME IT PASSES THROUGH ZERO. AMPLITUDE SCALING OF THE COSINE TRIANGLE IS ACCOMPLISHED BY EXACT MATCH OF THE INTEGRATING CAPACITORS C17, C18, C19 AND C20 WITH THEIR COUNTERPARTS IN THE SIN INTEGRATOR. ZERO DC LEVEL IS HELD BY INTEGRATING THE OUTPUT OF A5 THROUGH A5 ON BOARD 9 AND FEEDING IT BACK TO THE PLUS INPUT OF A5.

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5.11 - 'X5' INTEGRATE

REFERENCE: DRAWING NO. C103306-1

5.11.1 - FUNCTIONS

THE 'X5' INTEGRATE BOARD PERFORMS THREE FUNCTIONS:

1) SETS UP LOGIC COMBINATIONS NECESSARY FOR THE TIMING OPERATION.

2) ESTABLISHES INTEGRATE (OPERATE) TIME THAT IS A FIXED PERCENTAGE OF ALL TIME FOR OPERATION IN THE LOWEST FREQUENCY RANGES.

3) RESTRAINS FREQUENCY RANGE SWITCHING FROM FR2 TO 3 TO CERTAIN CONDITIONS OF THE TRIANGLE.

4) PREVENTS DOUBLE AUTOMATIC GAIN CONTROL ACTION WHEN A NOISE OVERLOAD COMBINES WITH A SIGNAL O.L.

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5.11.2 - OVERLOAD LOGIC UL1, UL4

UL1, UL4 COMBINE THE AUTOMATIC GAIN CONTROL FUNCTIONS THAT ARE NOT INCLUDED ON THE AUTOMATIC GAIN CONTROL BOARD #5.

UL4 IS DRIVEN BY THE 'RESET' SIGNAL FROM THE TIMING BOARD. UL4 GENERATES A PULSE AT THE START OF THE 'RESET' PERIOD WHICH IS USED BY THE AUTOMATIC GAIN CONTROL BOARD TO TIME THE GAIN CHANGE DUE TO SIGNAL OVERLOAD AND SIGNAL UNDERLOAD, AND CAUSE THEM TO OCCUR ONLY DURING THIS PERIOD, LEAVING THE REMAINING PORTION OF RESET TIME FOR SETTLING OUT FROM THE GAIN CHANGE. NOTE TOO, THAT THIS TIME IS AFTER THE NEW RESULT HAS BEEN READ INTO THE OUTPUT. ALL READING TRANSIENTS HAVE ENDED, BEFORE THE GAIN CHANGE DECISIONS ARE MADE.

UL4 HAS TWO ONE-SHOTS IN SERIES. THE SECOND ONE-SHOT CAN BE INHIBITED BY THE PRESENCE OF A 'S+N' OVERLOAD. THIS GIVES PRIORITY TO THE NOISE OVERLOAD RESPONSE AND ASSURES THAT A TWO STEP GAIN CHANGE DOES NOT OCCUR WHEN BOTH SIGNAL AND 'S+N' OVERLOADS ARE PRESENT SIMULTANEOUSLY.

PIN '9' RECEIVES THE (S+N) OVERLOAD PULSE OF CH#1 FROM BD.#5. EITHER OF THESE INPUTS GOING TO GROUND, DRIVES ITS RESPECTIVE -1 AMPLIFIER UL1C OR UL1A OUTPUT TO -15, AND INHIBITS THE SECOND ONE-SHOT OF UL4 BY TAKING 13 OF UL4 TO -15 (THRU 'OR' GATE CR3, CR2, R2).

UL5B GENERATES A PULSE TO PIN 'N' FOR EITHER CHANNEL (S+N) OVERLOAD. IT DRIVES TIMING BOARD TO 'RESET' AND ABORTS CYCLE OF ANALYSIS.

THE REMAINING INVERTERS OF UL1 DRIVE THE OVERLOAD LIGHTS ON THE FRONT PANEL. FOR CH#1, CR4, R19, C2, STRETCH THE OVERLOAD PULSE AND DRIVE UL1 OUTPUT TO GROUND. THE 'OR' GATE CR18, R12, CR17, RESPONDS TO THIS (S+N) OVERLOAD INPUT, OR THE SIGNAL OVERLOAD INPUT FROM BD#12 TO PIN 'D' AND CR17. IT DRIVES UL1 OUTPUT TO -15 AND ENERGIZES THE OVERLOAD LIGHT CH#1.

THUS, THE OVERLOAD LIGHT GOES 'ON' FOR A WHOLE CYCLE OF ANALYSIS DUE TO A SIGNAL OVERLOAD, OR FOR A SHORT TIME DUE TO A (S+N) OVERLOAD.

FOR CH#2, CR1, R18, C1, STRETCH THE (S+N) OVERLOAD INPUT. UL1B INVERTS IT. CR16, R11, CR15 FORM AN 'OR' GATE DRIVEN BY (S+N) OVERLOAD FROM UL1B, OR SIGNAL OVERLOAD FROM PIN '4', (FROM BD#12) TO ENERGIZE CH#2 OVERLOAD LIGHT, (UL1D OUTPUT GOING NEGATIVE TO PIN '5' AND THEN TO LEFT HAND CABLE).

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5.11.3 - 'X5' INTEGRATE

THE ANALYZER MAY BE COMMANDED INTO 'X5' INTEGRATE BY S15 ON FRONT PANEL THRU PIN 'W', CR19, R15, UL5D TO PIN '14'; OR FROM THE REAR PANEL J102-11 AT -15 VOLTS TO PIN '15', CR20, R13, UL5D TO PIN '14'.

UL5E GENERATES $\overline{\text{'X5'}}$ AS ANOTHER NECESSARY LOGIC LEVEL FOR THE ANALYZER.

5.11.4 - MISCELLANEOUS LOGIC LEVELS

F.R. (3+4) AND F.R. (5+6) COMMANDS ARE BROUGHT IN FROM THE EXTENDED SWEEP BOARD #2. UL6B 'OR' GATE DETERMINES F.R. (1+2) AND THE INVERTER UL5 GENERATES F.R. (1+2). THESE ARE USED IN DC/FREQUENCY, TIMING, ETC.

UL6A 'OR' GATE IS USED TO ESTABLISH $\overline{[(1+2)+(X5)]}$, AND UL6D 'OR' GATE FOR $[\overline{(1+2)}+(X5)]$. THESE ARE USED ON THE TIMING BOARD.

5.11.5 - FREQUENCY RANGE SWITCHING - UL5C, UL5A & UL6C. FREQUENCY RANGE 2 TO FREQUENCY RANGE 3

FREQUENCY RANGE SWITCHING FROM F.R.2 TO F.R. 3 MUST BE DELAYED UNTIL THE TRIANGLE IS MOVING IN A PLUS SENSE.

AT THIS TIME, THE SQUARE WAVE IS -15 VOLTS. THE LOGIC CAUSES PIN '21' TO BE -15, AND PERMITS NORMAL SWITCHING.

IF F.R. 2 IS PRESENT AND THE SQUARE WAVE IS PLUS, PIN '21' IS AT GROUND, AND THE SWITCHING IS INHIBITED UNTIL THE SQUARE WAVE GOES MINUS. (THE SWEEP IS IN 'HOLD' AT 100% F.S. FOR AT MOST 1/2 CYCLE OF 1 HZ).

IF FREQUENCY RANGE IS OTHER THAN '2', PIN '21' STAYS AT -15 REGARDLESS OF THE SQUARE WAVE'S POLARITY. IMMEDIATE FREQUENCY RANGE SWITCHING OCCURS AT THE 100% F.S. FREQUENCY. NOTE PIN 'P' IS THE INVERTED SQUARE WAVE AT '0' TO -15 VOLTS LOGIC LEVEL.

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5.11.6 - OPERATE-HOLD TIMING
UL2, UL3, UL7, UL8, CR5, 6, 7, 8, 14, R4 'OR' GATE

THE LOGIC FOR GENERATING AND SELECTING THE OPERATE-HOLD COMMANDS TO THE INTEGRATORS OF BOARDS #7 AND #8, IS CONTAINED IN THE ABOVE DIGITAL LOGIC ELEMENTS.

THE 7 KHZ SIGNAL IS BROUGHT IN AND COUNTED DOWN 4/1 BY UL8. IT THEN BECOMES THE INPUT TO UL7, A DECADE COUNTER DIVIDER. EACH OUTPUT IS 'ON' 1/10TH OF THE TIME AT 176 TIMES PER SECOND. THE COUNT OF 4 WAS SELECTED.

THE BINARY COUNTER UL8 HAS A SECOND OUTPUT DOWN 4/1 FROM THAT WHICH DRIVES UL7.

THESE TWO OUTPUTS DRIVE THE 'AND' GATE CR13, CR12, R9. CONSIDER WHEN BOTH INPUTS ARE AT GROUND (THE 'ON' CONDITION) SIMULTANEOUSLY. COUNTING PULSES FROM PIN '4' OF UL8, PIN '10' OF UL7 WHICH HAVE A GROUND OUTPUT AT THE 4, 14, 24, 34TH PULSE. PIN '6' OF UL8 IS AT GROUND ON THE 4, 8, 12, 16, 20, 24, 28, 32, 36TH PULSE. EVERY OTHER PULSE FROM UL7 OCCURS WHEN UL7 INPUT IS AT GROUND, AND THE OTHER WHEN IT IS AT -15. THE NET OUTPUT AT R9, IS AN 'ON' COMMAND 1/20TH OF THE TIME.

THE OUTPUT AT PIN '11' OF UL8 IS USED AS 1/2 'ON', 1/2 'OFF' COMMAND.

THE OUTPUT OF PIN '10' OF UL8 BECOMES THE INPUT TO THE TIMING BOARD FOR TIMING FREQUENCY RANGE (5+6).

IN FREQUENCY RANGES 3, 4, 5, 6, THE OPERATE - 'HOLD' COMMAND IS SET BY THE TIMING BOARD ONLY. CR14 IS GROUNDED BY UL6B OUTPUT. UL3 TRANSMITS THE INPUT FROM PIN '2' TO OUTPUT PIN '3' TO INTEGRATORS.

IN FREQUENCY RANGE 2 (PIN 'V' AT GROUND), AND '$\overline{X5}$', UL3C OUTPUT IS GROUND. CR8 GROUNDS PIN '12' OF UL3D AND OPERATION IS IDENTICAL WITH FREQUENCY RANGES 3, 4, 5 & 6.

IN FREQUENCY RANGE 2, AND 'X5', UL2C OUTPUT IS GROUND, UL3B RESPONDS TO THE '1/2' TIME 'ON-OFF' COMMAND FROM PIN '11' OF UL8. THIS MODULATES THE OPERATE-HOLD COMMAND TO UL3D AS UL3B BRINGS CR7 TO GROUND 1/2 OF THE TIME. J1 WILL SHOW A BALANCED 'ON-OFF' SQUARE WAVE AT 220 HZ DURING THE OPERATE TIME.

IN FREQUENCY RANGE 1, PIN '10' IS GROUND. WITH 'X5', UL2A OUTPUT IS GROUND. UL2D FOLLOWS THE 1/10TH ON COMMAND FROM PIN '10' OF UL7 AT 176 'ON' TIMES/SEC. THIS, IN TURN THRU CR5, MODULATES THE OPERATE TIME 'ON' COMMAND TO REDUCE THE 'ON' TIME TO 1/10TH TOTAL OPERATE TIME.

AGAIN, IN FREQUENCY RANGE #1, IN 'X5', UL2B OUTPUT IS AT GROUND, UL3A PASSES THE 1/20TH 'ON' TIME PULSES AT 88/SEC. TO DRIVE CR6. UL3D OUTPUT HAS THE OPERATE TIME MODULATED FOR 1/20TH TOTAL OPERATE TIME BEING 'ON' WITH THE 'ON' SAMPLES AT 88/SEC.

NOTE THAT THIS SELECTION AND TIMING IS AUTOMATIC.

5.11.7 - ADJUSTMENTS & TEST POINTS

THERE ARE NO ADJUSTMENTS ON THIS BOARD.

J0 - GROUND

J1 - 'COMMAND TO INTEGRATORS' HOLD-OPERATE. SHOWS TIMING AND SHOWS 1/2, 1/10, 1/20 SAMPLING.

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5.12 - AMPLITUDE (DB) AND AMPLITUDE RATIO

REFERENCE: DRAWING NO. C103395
& SEC. 4.7.2 - THEORY

5.12.1 - FUNCTIONS

BOARD #12 HAS THE AMP CH#1 AND AMP CH#2 AS INPUTS FROM PHASE AND AMP BOARDS #13 AND #14.

1) IT DETERMINES IF AMP CH#1 OR CH#2 IS AN OVERLOAD AND GENERATES SIGNAL OVERLOAD LOGIC LEVELS.

2) IT DETERMINES IF AMP CH#1 OR CH#2 IS AN UNDERLOAD AND GENERATES SIGNAL UNDERLOAD LOGIC LEVELS.

3) COMPUTES LOG AMP OF AMPLITUDE INPUT AND ADDS LOG GAIN TO GIVE NET AMPLITUDE IN DB FOR CH#1 AND CH#2, RESPECTIVELY.

4) SUBTRACTS DB AMP CH#1 FROM DB AMP CH#2 TO GIVE AMPLITUDE RATIO IN DB.

5) PERFORMS READ-HOLD OF THE RESULTS TO SYNCHRONIZE WITH THE ANALYZER OPERATION.

6) DETERMINES A LOGIC LEVEL INDICATING

$$\overline{UL1} + \overline{UL2} + \overline{OL1} + \overline{OL2} .$$

AS TWO CHANNELS OF COMPUTATION ARE PRESENT ON THIS BOARD, CH#1 WILL BE DESCRIBED WITH PARENTHESES FOR THE EQUIVALENT COMPONENTS OF CH#2.

5.12.2 - SIGNAL OVERLOAD DETERMINATION AMP 1A, (AMP 2A)

AMP 1A (2A) IS THE CH#1 (CH#2) SIGNAL OVERLOAD DETECTOR. WHEN THE AMPLITUDE INPUT FROM THE PHASE AND AMPLITUDE COMPUTER IS UNDER +5.0 VOLTS, AMP 1A (AMP 2A) OUTPUT IS -12 VOLTS. WHEN THE AMPLITUDE INPUT IS GREATER THAN +5.0 VOLTS, AMP 1A (AMP 2A) OUTPUT IS +12 VOLTS. PIN 'K' ('N') IS LIMITED TO +.7 VOLTS BY R9, CR1 (R18, CR3). THIS IS THE SIGNAL OVERLOAD LINE TO THE AUTOMATIC GAIN CONTROL BOARD.

5.12.3 - SIGNAL UNDERLOAD DETERMINATION
AMP 1B, Q1 (AMP 2B, Q2)

AMP 1B (2B) IS THE CH#1 (CH#2) SIGNAL UNDERLOAD DETECTOR. WHEN THE AMPLITUDE FROM THE RESPECTIVE PHASE AND AMP BOARD IS LESS THAN 1.25 VOLTS, AMP 1B (AM2B) OUTPUT IS -12 VOLTS. Q1 (Q2) IS DRIVEN 'ON'. THE NET OUTPUT AT PIN 'M' ('Y') IS AN UNDERLOAD INDICATION OF -.7 VOLTS.

WHEN THE AMPLITUDE INPUT IS GREATER THAN 1.25 VOLTS, AMP 1B (2B) OUTPUT IS +12 VOLTS, Q1 (Q2) IS DRIVEN 'OFF'. PIN 'M' ('Y') IS AT -15 VOLTS INDICATING NO SIGNAL UNDERLOAD.

5.12.4 - FLAG - $\overline{\text{READ}}$ -

PIN 'S' IS A $\overline{\text{READ}}$ FLAG. WHEN AT -12 TO -15 VOLTS, THERE IS NO SIGNAL OVERLOAD OR UNDERLOAD IN EITHER CHANNEL, AND A NEW RESULT IS NOT BEING READ IN. PIN 'P' IS ENERGIZED BY THE 'READ-HOLD' COMMAND.

PIN 'S' IS AT GROUND, IF THERE IS A SIGNAL OVERLOAD OR A SIGNAL UNDERLOAD IN EITHER CHANNEL, OR WHILE A NEW RESULT IS BEING READ INTO THE OUTPUT.

J102-8 HAS THIS FLAG.

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5.12.5 - AMPLITUDE - DB -

THE AMPLITUDE INPUT IS CONVERTED TO A DC VOLTAGE PROPORTIONAL TO LOG AMPLITUDE BY UL1, Q3, UL3A (UL2, Q4, UL3B).

THE BASIC LOG CONVERSION IS ACCOMPLISHED BY A TRANSISTOR IN THE FEEDBACK OF AN AMPLIFIER AS Q3A AROUND UL1A (Q4A AROUND UL2A). THE TRANSISTOR IS PART OF AN I.C. PACKAGE WITH A TEMPERATURE CONTROLLED SUBSTRATE. THIS REDUCES THE EFFECT OF TEMPERATURE DRIFT ON THE CALIBRATION.

A SECOND LOG CONVERSION IS INTRODUCED BY A FIXED INPUT TO UL1B (UL2B) WITH Q3B (Q4B) IN THE FEEDBACK. THIS OUTPUT IS SUBTRACTED FROM THE FIRST IN UL3A (UL3B). THE HIGH COMMON MODE REJECTION - DC LEVEL IN THIS CASE - FURTHER REDUCES THE EFFECT OF TEMPERATURE DRIFT BY SUBTRACTING THE DRIFT TERM. THUS, EVEN DURING WARMUPS, THE RESULTS ARE MUCH LESS EFFECTED BY TEMPERATURE.

R28 (R37) SET THE FIXED OUTPUTS OF UL1B (UL2B). IT IS NORMALLY ADJUSTED FOR ZERO VOLTS AT UL3A (UL3B) OUTPUT WHEN THERE IS 5.00 VOLTS AMPLITUDE - PINS 'L' ('R'). IN USE, R28, R59 (R37, R60) ARE ADJUSTED FOR ZERO, AND SPAN AT 0.5 AND 5.0 VOLTS INPUT - SEE SEC. 6.8.

5.12.6 - OUTPUT - 'READ-HOLD' - A3, (A4), Q5, (Q6)

AMP 3 (4) IS PUT IN 'HOLD' WHEN Q5 (Q6) IS 'OFF'.

AMP 3 (4) FOLLOWS A NEW INPUT WHEN Q5 (Q6) IS 'ON'. THIS IS COMMANDED BY THE TIMING BOARD.

THE INPUT TO AMP 3 (4) IS THE SUM OF THE LOG CONVERSION OF AMPLITUDE FROM UL3A (UL3B), AND THE LOG OF GAIN ON PIN '6' (PIN '20') AS COMPUTED BY THE RESPECTIVE INPUT AMPLIFIER.

R59 (R60) PERMITS A PRECISE SCALING OF LOG AMPLITUDE.

THE NET OUTPUT IS 'DB AMPLITUDE' OF THE FUNDAMENTAL COMPONENT OF THE RETURN SIGNAL FOR CH#1 ON PIN '4' AND J1, AND FOR CH#2 ON PIN '21' AND J2. THE SCALING IS 2 VOLTS/20 DB. THE RANGE IS +20 DB TO -60 DB.

5.12.7 - AMP RATIO - A5 - DB

A5 SUBTRACTS THE DB CH#1 FROM DB CH#2 TO GIVE AN OUTPUT OF AMPLITUDE RATIO CH#2/CH#1 IN DB.

A5 DOES NOT NEED A SEPARATE 'READ-HOLD' CIRCUIT AS BOTH OF TIS INPUTS ARE ACTING IN UNISON.

AMP RATIO IN DB IS ON PIN '3' AND TEST POINT #3 AT 2 VOLT/20 DB OVER ±80 DB. ZERO DB = ZERO VOLTS = RATIO OF 1/1.

5.12.8 - ADJUSTMENTS & TEST POINTS

J0	-	GROUND
J1	-	AMP CH#1 IN DB - 2.0 VOLT/20 DB.
J2	-	AMP CH#2 IN DB - 2.0 VOLT/20 DB. ZERO DB = 8.0 VOLT PEAK
J3	-	AMP RATIO CH#2/CH#1 IN DB 2 VOLT/20 DB; ZERO VOLT = RATIO OF 1/1
R28	-	ZERO DB CH#1 ADJUSTMENT
R37	-	ZERO DB CH#2 ADJUSTMENT

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5.13 & 14 - PHASE & AMPLITUDE - BOARDS #13 & #14

REFERENCE: DRAWING NO. C103401-1;-2
SECTION 4.7.1 - THEORY

5.13 & 14.1 - FUNCTIONS

THE PHASE AND AMPLITUDE BOARD #13 PERFORMS THE FOLLOWING FUNCTIONS:

1) MODULATE THE IN-PHASE AND QUADRATURE COMPONENTS OF CH#1 MULT-INT (BD. #7) AT 7 KHZ. THE QUADRATURE MODULATION IS 90° PHASE SHIFTED FROM THE IN PHASE MODULATION.

2) AMPLIFIES AND FILTERS THE SUM OF THE MODULATED SIGNALS.

3) GENERATES A SQUARE WAVE AT THE ZERO CROSSINGS OF THE FILTERED SIGNAL.

4) COMPUTES AMP CH#1 FROM THE INVERTED SQUARE WAVE OF STEP 3 (7 KHZ BOARD).

5) PARTICIPATES IN PHASE SHIFT COMPUTATION.

NOTE THE PHASE AND AMPLITUDE BOARD PERFORMS ITS COMPUTATION DURING THE 'OPERATE' PORTION OF THE TIMING, BUT SETTLES OUT AND GIVES A PRECISE RESULT DURING THE FIRST PART OF THE 'HOLD' PERIOD.

THE TWO PHASE AND AMPLITUDE BOARDS #13 AND #14 ARE IDENTICAL IN ALL RESPECTS EXCEPT THE PHASE SHIFT OUTPUT, A5. BOTH BOARDS ARE DESCRIBED WITH EQUIVALENT NOTATIONS OF BOARD #14 IN PARENTHESIS WHERE NECESSARY.

THE SECTION IN PHASE SHIFT 5.13 (14).6 TAKES EACH BOARD IN TURN TO SHOW HOW THE FINAL PHASE SHIFT IS OBTAINED.

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5.13 & 14.2 - MODULATION AT 7 KHZ

THE IN-PHASE INTEGRATOR OUTPUT OF BOARD #7 (8) DRIVES PIN 'B'. Q3 IS DRIVEN 'ON' AND 'OFF' BY THE 7 KHZ SQUARE WAVE AT 0° REFERENCE PHASE. THE CURRENT THRU R9 IS PROPORTIONAL TO THE AMPLITUDE OF THE IN-PHASE INPUT FROM THE CH#1 (CH#2) INTEGRATOR, AND THE CURRENT IS A SQUARE WAVE FROM GROUND TO THE INPUT (R4, R8, R9).

SIMILARLY, THE QUADRATURE INTEGRATOR DC OUTPUT IS MODULATED BY Q1 AT 7 KHZ. Q1 IS DRIVEN FROM THE 90° PHASE SHIFTED REFERENCE 7 KHZ SQUARE WAVE. THE CURRENT THROUGH R9 IS A SQUARE WAVE FROM GROUND TO INPUT (R1, R2) AT 90° TO THAT THRU R4, R8, R9. ITS AMPLITUDE (AND SENSE) IS PROPORTIONAL TO THE QUADRATURE INTEGRATOR OUTPUT OF BOARD #7 (8).

Q2 AND Q4 ARE TURNED 'ON' AND 'OFF' BY THE SAME SQUARE WAVES THAT DRIVE Q1 AND Q3. THEY HAVE THE SAME SPIKE FEEDTHROUGH AS Q1 AND Q3. THE SPIKES ARE ADJUSTED IN AMPLITUDE BY R6 AND R12 TO BE SUBTRACTED FROM THE NORMAL INPUTS TO IMPROVE THE NULL. (THEY GO TO THE PHASE INPUT OF A1).

5.13 & 14.3 - FILTERS - A1, A2

THE TWO COMPONENTS ARE ADDED IN A1 AND FILTERED BY R16 C5. THIS IS A SINGLE TIME CONSTANT EQUAL TO 22.5 MICROSECONDS, OR A BREAK FREQUENCY OF 7,080 HZ.

AMP 2 HAS A QUADRATIC LOW PASS RESPONSE. THE RESONANT FREQUENCY IS SET FOR 7030 HZ. THE DAMPING RATIO IS 0.35.

THE COMBINED FILTER REDUCES 3RD HARMONIC DISTORTION TO 1% AND HIGHER HARMONICS TO MUCH LESS.

AMP 1 OUTPUT HAS A DC LEVEL. THE HIGH PASS ACTION OF C7 R19 REMOVES THE DC LEVEL.

AMP 2 OUTPUT IS NOW GIVEN BY -

$$C = (\sin \omega t + \theta_F + \theta_1)$$

WHERE: $\theta_1 = \tan^{-1} \frac{\text{IN-PHASE}}{\text{QUAD}}$

θ_F = FILTER PHASE SHIFT AT 7030 HZ.

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5.13 & 14 .4 - SQUARING AT ZERO CROSSING A3, A6

A3 IS A FOLLOWER. ITS INPUT IS LIMITED BY THE DIODES CR6, CR7. THESE ARE VERY LOW CAPACITANCE DIODES WITH ±.3 VOLT LIMITING.

R55 PROVIDES A FINE ADJUST TO A2 TO BIAS OUT ANY OFFSET IN A2. THIS INSURES A BALANCED SINE WAVE OUT OF A2.

A3 DRIVES THE COMPARATOR A6. ITS LOW OUTPUT SWING PERMITS R70 TO BE ONLY 50 OHMS. THIS ELIMINATES THE EFFECT OF A6 INPUT CURRENT ON THE SQUARING ACTION.

A6 OUTPUT GOES FROM +10 VOLTS TO NEAR GROUND AND VICE VERSA AS THE INPUT GOES THRU ZERO IN ONE SENSE OR THE OTHER. THE VERY FAST ACTIVE PULL DOWN OF THE OUTPUT FROM +15 TO GROUND IS USED AS THE TRIGGER SIGNAL ON THE 7 KHZ BOARD.

Q11 INHIBITS THE COMPARATOR DURING THE 'RESET' MODE. IT PREVENTS OSCILLATION WHEN THE INPUTS - PIN 'L' AND 'B' ARE AT GROUND.

5.13 & 14.5 - AMPLITUDE CH#1 (2) - Q7, AMP 4, Q9

Q7 HALF WAVE, DEMODULATES THE OUTPUT OF A2. Q7 IS DRIVEN BY A SQUARE WAVE FROM THE 7 KHZ BOARD, ORIGINATING FROM A6 OUTPUT. THE PHASE (0,180) IS SUCH AS TO SELECT THE NEGATIVE PORTION OF A2 OUTPUT, TO GENERATE A PLUS OUTPUT OF A4.

THE HALF WAVE SIGNAL IS FILTERED BY R41, C15, R42. IT IS ALSO FILTERED BY C14, R44, R45 WHEN A4 IS IN 'READ'. THE NET RESULT IS A D.C. OUTPUT OF A4 DIRECTLY PROPORTIONAL TO THE AMPLITUDE OF THE SINE WAVE AT A2 OUTPUT, OR IN TURN OF THE $(\text{IN-PHASE}^2 + \text{QUADRATURE } 2)^{1/2}$ OF THE INPUTS.

R54 SETS THE 10% OUTPUT TO COMPENSATE FOR THE OFFSET DUE TO SWITCHING SPIKES.

Q9, C14 PROVIDES THE 'READ-HOLD' ACTION AS COMMANDED FROM TIMING BOARD. THE OUTPUT IS SCALED FOR +5.00 VOLTS FULL SCALE.

R44 SPANS THE AMPLITUDE READOUT.

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5.13 & 14.6 - PHASE SHIFT

THE PHASE SHIFT OUTPUT USES A5 ON BOTH BOARDS #13 AND #14, AS FOLLOWS:

BOARD #14 -

Q8 IS DRIVEN BY THE PHASE SQUARE WAVE WHOSE 'ON' TIME AS A FRACTION OF 'CYCLE' TIME IS PROPORTIONAL TO PHASE SHIFT.

THE COMMON OF R64, R51 , ASSUMES A D.C. LEVEL PROPORTIONAL TO PHASE.

A5 AMPLIFIES AND FILTERS (C16, R46), THE INPUT (NO 'READ-HOLD' ACTION).

R59 PROVIDES A BIAS TO ASSIST IN MAKING ZERO PHASE CORRESPOND TO 1/2 'ON', 1/2 'OFF TIME OF Q8.

BOARD #13 -

THE INPUT ON PIN 'C' IS THE OUTPUT OF A5 BOARD #14.

R50 PROVIDES A PRECISE ZERO ADJUST.

Q10, C16 PROVIDE A 'READ-HOLD' ACTION. A5 OUTPUT IS SCALED TO ±9.0 VOLTS FOR ±180°. R47 IS THE SPAN ADJUST.

R72, R71 SCALE THE OUTPUT DOWN TO ±1.80 VOLTS FOR ±180°. THIS IS SET PRECISELY USING R47.

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5.13 & 14.7 - ADJUSTMENTS & TEST POINTS COMMON TO BOARDS #13 & #14

TEST POINTS:

J0	-	GROUND
J1	-	AMPLITUDE - +5.0 VOLTS F.S. BOARD #13 - CH#1; BOARD #14 - CH#2

ADJUSTMENTS:

R55	-	ZERO ADJUST OF SQUARING ACTION.
R54	-	10% AMPLITUDE ADJUSTMENT
R44	-	100% AMPLITUDE SPAN

BOARD #13 ONLY:

J2	-	PHASE SHIFT - ±1.80 VOLTS.
R50	-	PHASE ZERO
R47	-	PHASE SPAN

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5.15 - 7KHZ

REFERENCE: DRAWING NO. 103046
& SEC. 4.7 & 4.9.1 FOR THEORY

5.15.1 - FUNCTION

1) THE 7KHZ BOARD ESTABLISHES THE SQUARE WAVES AT 90° PHASE SEPARATION FOR THE PHASE AND AMPLITUDE COMPUTER.

2) THE ATTENUATION CONTROL SYSTEM IS INCLUDED.

3) THE PHASE SHIFT IS DETERMINED FROM THE SQUARED OUTPUTS OF THE PHASE AND AMP BOARD TO THE SIGNAL TO DRIVE THE PHASE SHIFT FET ON BOARD #13.

SEE SEC. 4.9.1 FOR THEORY OF ATTENUATION CONTROL.
SEE SEC. 4.7 FOR PHASE SHIFT AMPLITUDE COMPUTATION.

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5.15.2 - 7 KHZ GENERATION

AMP 1, AMP 2, Q1, Q2, CR10 THRU CR14 -

AMP 1 IS AN INTEGRATOR. AMP 2 IS A COMPARATOR. AMP 2 OUTPUT AT ±13 VOLTS DRIVES THE DIODE SWITCHING NETWORK CR10, 11, 12, 13, TO PASS CURRENT THRU ZENER DIODE CR14 IN THE SAME SENSE. THIS GIVES NEAR IDENTICAL PLUS AND MINUS LEVELS AT THE COMMON OF R40, R25.

THE LOOP IS CONNECTED WITH POSITIVE FEEDBACK. WHEN A2 OUTPUT IS '+', A1 IS INTEGRATING DOWN. WHEN A1 OUTPUT EXCEEDS THE +8 VOLT REFERENCE, A2 FLIPS TO '-' OUTPUT. THE REFERENCE BECOMES '-8' VOLTS, A1 INTEGRATES UP, ETC.

THE OUTPUT OF A1 IS A TRIANGLE OF ±8 VOLT SWING AND BALANCED IN ITS PLUS AND MINUS GOING SENSE.

A2 OUTPUT IS A SQUARE WAVE SWITCHING WHEN A1 TRIANGLE REACHES ITS PEAKS.

FREQUENCY IS STABILIZED BY THE COMMON SOURCE FOR REFERENCE TO THE INTEGRATOR AND TO THE COMPARATOR, AND BY THE COMPONENT SELECTION.

UL1F SHARPENS THE RISE AND FALL TIMES, AND GIVES THE DESIRED GROUND TO -15 VOLT LEVELS TO DRIVE THE FETS.

AMP 3 ACTS AS A ZERO CROSSING DETECTOR. R13, C5, R12 ARE POSITIVE FEEDBACK FOR FASTER SWITCHING ACTION. THE SQUARE WAVE OUTPUT CORRESPONDS IN TIME TO THE ZERO CROSSING OF THE SQUARE WAVE. THUS, IT IS PRECISELY 90° OUT-OF-PHASE WITH A2 OUTPUT. C25 IS SELECTED TO MAKE THE 90° PHASE SHIFT MORE PRECISE.

UL1E SHARPENS THE SQUARE WAVE AND SETS IT TO ZERO TO -15 VOLTS TO DRIVE THE FETS ON THE PHASE AND AMP BOARDS.

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5.15.3 - ATTENUATION CONTROL

A4, UL1C, Q3, Q4, A5 - SEC. 4.9.1 FOR THEORY

THE COMPARATOR A4 HAS THE 7KHZ TRIANGLE AND A DC INPUT. THE DC INPUT DETERMINES THE PULSE WIDTH OF A4 OUTPUT. UL1C SQUARES THE A4 OUTPUT FURTHER AND DRIVES Q3 'ON' AND 'OFF'. THE RATIO OF 'ON' TIME TO TOTAL TIME (PER CYCLE) DETERMINES THE DC LEVEL TO A5 THRU R42, R44. DCS1 THRU R18, R45 DETERMINES THE SECOND DC INPUT.

AMP 5 INTEGRATES THE DIFFERENCE AND CONTINUOUSLY CHANGES THE PULSE WIDTH OUT OF A4 TO KEEP THEM IN PRECISE BALANCE. THE AUTOMATIC BALANCE MAKES THE FET SWITCHING PRODUCE AN ATTENUATION (OF -15 VOLTS) DIRECTLY PROPORTIONAL TO DCS1 (OR FREQUENCY). THUS, AT FULL SCALE (DCS1 = 10 VOLT), ATTENUATION = .90; AT 10% OF FULL SCALE, ATTENUATION = .09. THIS DIRECTLY COMPENSATES FOR THE LONGER INTEGRATE TIME AT THE LOW FREQUENCY END OF EACH FREQUENCY RANGE.

AS A4, R42, R44 ARE SIMILAR TO THE MULTIPLIER ATTENUATION CIRCUIT, THE OUTPUT AT TE 'Z' CAN DRIVE THE MULTIPLIER ATTENUATOR FETS IN SUCH A MANNER AS TO GIVE EACH ONE THE IDENTICAL ATTENUATION LINEARLY PROPORTIONAL TO DCS1.

Q4 IS 'OFF' IN THE FREQUENCY RANGES 1 THRU 4. IN THE TWO HIGH FREQUENCY RANGES, Q4 IS 'ON'. THIS INPUT TO A5 THRU R50 COMMANDS THE ATTENUATION FETS AS 'OFF' (NO ATTENUATION). (INTEGRATE TIME IS FIXED IN FREQUENCY RANGES 5 & 6).

R18 SPANS THE ATTENUATION AS 9% TO 90%. R51 SETS THE LOW END (9%) TO ALLOW FOR ANY OFFSETS.

R57, C24, R17 ASSIST IN FILTERING THE INTEGRATOR OUTPUT TO FURTHER ATTENUATE THE 7KHZ TERM LEFT FROM THE INTEGRATION OF THE ATTENUATED SIGNALS.

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5.15.4 - PHASE COMPUTER - UL1A, UL1B, UL3, UL2

THE SQUARE WAVE OUTPUT (ZERO TO +15 VOLTS FROM BOARD #13) OF THE CH#1 PHASE AND AMP BOARD IS LEVEL SHIFTED BY R2, R1 AND THE BYPASS EFFECT OF C1. UL1B IS DRIVEN FROM -2.5 TO -12.5 VOLTS. UL1B SQUARES THE INPUT FURTHER AND TRIGGERS ONE OF THE ONE-SHOTS OF UL2.

UL1B OUTPUT IS INVERTED BY UL3D AND DRIVES THE AMPLITUDE FET OF BOARD #13.

IN THE SAME WAY, THE SQUARE WAVE OUTPUT OF CH#2, BOARD #14, PHASE AND AMPLITUDE IS LEVEL SHIFTED BY R3, R4, BY-PASSED BY C3 AND DRIVES UL1A. THE OUTPUT OF UL1A TRIGGERS THE SECOND ONE-SHOT OF UL2, AND IT DRIVES THE INVERTER UL3C. THE OUTPUT OF UL3C IS USED ON BOARD #14 TO DETERMINE AMPLITUDE CH#2.

THE TWO PULSES OUT OF UL2 OCCUR AT THE ZERO CROSSING OF THE RESPECTIVE 7KHZ SINEWAVE IN THE PHASE AND AMP BOARD. THE SEPARATION OF THESE PULSES IS PROPORTIONAL TO PHASE SHIFT.

UL3A, UL3B ARE CONNECTED AS A FLIP-FLOP. THE PULSES SET AND RESET THE FLIP-FLOP. THE 'ON-TIME' AS A FRACTION OF TOTAL TIME, IS THE PHASE SHIFT OVER 360°. UL1D BUFFERS THE OUTPUT TO DRIVE THE PHASE FET ON BOARD #13.

5.15.5 - ADJUSTMENTS & TEST POINTS

FRONT

R51 - LINEARITY OF ATTENUATION AT LOW END OF FREQUENCY RANGE. (SEE SEC. 6.5).

R19 - FREQUENCY - 7KHZ - AT J1 - SET FOR 7030 HZ.

INSIDE

R18 - SPAN OF ATTENUATION CIRCUIT.

J0 - GROUND
J1 - TRIANGLE AT 7030 HZ.
J2 - ATTENUATOR OUTPUT - 0 TO -15 VOLTS.

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5.16 - TIMING BOARD

REFERENCE: DRAWING NO. C103314
& SECTION 4.6 - THEORY: FIG. 4.6-1

5.16.1 - FUNCTIONS

1) THE TIMING BOARD SETS THE 'OPERATE' TIME AS A FUNCTION OF FREQUENCY, FREQUENCY RANGE, AND 'X5' 'IN' OR 'OUT'.

2) IT SEQUENCES 'HOLD' AND THEN 'RESET' MODES FOLLOWING 'OPERATE'.

3) IT INTERLOCKS WITH NOISE OVERLOAD, FREQUENCY RANGE SWITCHING, END OF SWEEP, ON-OFF SWITCHING IN SUCH A WAY AS TO PREVENT AN INCORRECT RESULT FROM ENTERING THE READOUTS.

5.16.2 - FREQUENCY RANGES 1, 2, 3 & 4 - OPERATE TIME - UL1, UL3, UL4

THE PULSES REQUIRED FOR THE TIMING OF FREQUENCY RANGES 1, 2, 3 & 4 ARE OBTAINED FROM THE TEST FREQUENCY BY UL1. FOUR PULSES PER CYCLE ARE GENERATED.

UL1 - EXCLUSIVE OR GATE - QUAD

UL1-D - SQUARES THE SINE WAVE REFERENCE DRIVING PIN '5'. THE ACTION IS THAT OF A LEVEL DETECTOR WITH POSITIVE FEEDBACK (SCHMIDT TRIGGER).

UL1-A - GENERATES A PULSE AT EVERY ZERO CROSSING OF THE INPUT SQUARE WAVE. R2 C1 SET THE PULSE WIDTH.

UL1-B - GENERATES A PULSE AT EVERY ZERO CROSSING OF THE SQUARED SINE WAVE AT UL1-D OUTPUT. R5 C2 SET THE PULSE WIDTH.

UL1-C - DELIVERS A PULSE OUTPUT FOR EACH NON-COINCIDENT PULSE INPUT.

THE NET RESULT AT J1 IS A TRAIN OF PULSES AT 4 PULSES PER CYCLE OF THE TEST FREQUENCY.

UL2-A - TRANSMITS THE PULSES FROM UL1 TO UL3 IN FREQUENCY RANGES 1, 2, 3 & 4.

UL3 DIVIDES THE PULSE TRAIN BY 1, 2, OR 4 AS FOLLOWS:

IN F.R. 1, 2, 3 & 4 WHEN 'X5' ('X5' OUT), BY '1'.

IN F.R. (1 + 2) WHEN 'X5' 'IN', BY '2'.

IN F.R. (3 + 4) WHEN 'X5' 'IN', BY '4'.

UL3 IS IN RESET COUNT DURING 'HOLD' AND 'RESET' ANALYZER MODES.

UL4 - DUAL BCD UP COUNTER

UL4 COUNTS THE INPUT PULSES FOR UL3 OUTPUT. IT HAS THREE OUTPUTS, AT PIN '5' - A PULSE EVERY 4 INPUT COUNTS AT PIN '6' - A PULSE EVERY 8TH INPUT COUNTS AFTER RESET. AT PIN '14' - A PULSE EVERY 80TH INPUT COUNT AFTER RESET.

UL8A, UL8B, UL2B, CR3, CR4, CR5, UL6A

END OF OPERATE TIME IS SELECTED AS FOLLOWS:

IN F.R. (1 + 2), UL8A RESPONDS TO THE UL4 COUNT OF 4 AND TRIGGERS THE UL6A ONE-SHOT THROUGH CR3.

IN F.R. 3, UL2B OUTPUT IS PLUS, AND UL8B RESPONDS TO THE UL4 COUNT OF '8' AND TRIGGERS THE UL6A ONE-SHOT THROUGH CR4.

IN F.R. 4, THE UL4 COUNT OF '80' GROUNDS CR5 AND TRIGGERS UL6A.

UL6A 'ON' TIME IS THE 'HOLD' MODE OF THE TIMING SEQUENCE.

UL6A OUTPUT RESETS THE UL3, AND UL4 CHAIN SO THAT EACH 'OPERATE' TIME AT THE SAME TEST CONDITION IS OF THE SAME TIME PERIOD.

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THE NET RESULT OF THE ABOVE IS THAT 4 PULSES PER CYCLE OF THE TEST FREQUENCY ACTING AS INPUT ARE COUNTED AND PRODUCE AN 'OPERATE' TIME EQUAL TO A WHOLE NUMBER OF CYCLES OF THE TEST FREQUENCY, AS FOLLOWS:

FREQUENCY RANGE	'X5' IN, OUT	PULSES COUNTED	# OF CYCLES OF TEST FREQUENCY
1	OUT	4	1
2	OUT	4	1
3	OUT	8	2
4	OUT	80	20
1	IN	8	2
2	IN	8	2
3	IN	40	10
4	IN	400	100

THIS ACTION IS AUTOMATIC AND EXACT. FURTHER, IT FOLLOWS FREQUENCY SWEEP.

5.16.3 - FREQUENCY RANGES (5 + 6) OPERATE TIME -

THE 'OPERATE' TIME IS A FIXED TIME IN FREQUENCY RANGES 5 AND 6.

220 HZ FROM THE 7 KHZ BOARD IS INTRODUCED AT PIN '9'. UL2C GATES IT AS AN INPUT TO UL3 IN THESE TWO FREQUENCY RANGES.

UL3 COUNTS IT DOWN BY 1 IN 'X5 OUT', AND BY 5 IN 'X5 IN'. UL4 COUNTS IT DOWN 8/1 TO TRIGGER UL6 THROUGH CR5.

THE 'OPERATE' TIME IS .036 SECONDS IN 'X5 OUT' - (8 CYCLES OF 220 HZ), AND .18 SECONDS IN 'X5 IN' - (40 CYCLES OF 220 HZ).

5.16.4 - OPERATE - READ-HOLD & OPERATE INTERLOCK TO RESET -

UL8C FOLLOWS THE COMMAND FROM UL6A WITH A TIME DELAY IN GOING 'ON' DETERMINED BY R19, C8. THE TIME DELAY PROVIDES A TIME BETWEEN THE START OF THE 'HOLD' MODE AND THE START OF 'READ' FOR THE PHASE AND AMP OUTPUT CIRCUITS. THIS DELAY ALLOWS THE PHASE AND AMP COMPUTATION TO SETTLE OUT BEFORE IT IS READ.

UL6A (PIN '7' TO PIN '13' OF UL6B) INHIBITS THE ACTION OF THE RESET ONE-SHOT. THIS PREVENTS RESET FROM BEING TRIGGERED UNTIL 'HOLD' IS COMPLETED. THUS, THE RESULTS OF A SATISFACTORY CYCLE OF ANALYSIS ARE ALWAYS READ CORRECTLY INTO THE OUTPUT, ONCE THEY HAVE GONE INTO 'HOLD'.

5.16.5 - RESET - UL6B, UL7A

AT THE END OF 'HOLD', UL6B IS TRIGGERED BY UL5A. THE DELAY DUE TO R20 C9 IS ESSENTIAL TO ALLOW UL6B TO RECOVER FROM THE INHIBIT COMMAND TO PIN '13'.

UL6B 'SETS' THE UL7A FLIP-FLOP SO THAT 'RESET' IS COMMANDED AT PIN 'L' BY UL5D. UL6B ESTABLISHES THE MINIMUM 'RESET' TIME. THE UL3, UL4 CHAIN ARE ALSO KEPT IN 'RESET' THRU CR22.

AFTER UL6B RETURNS TO ITS NORMAL STATE, UL7A MAINTAINS THE ANALYZER IN 'RESET' UNTIL THE NEXT PULSE THROUGH UL8D RESETS THE FLIP-FLOP, AND TAKES THE ANALYZER OUT OF 'RESET' MODE. A SUFFICIENT DELAY IS BUILT IN (R7, C3), SO THAT THE RELEASE PULSE IS NOT COUNTED. THUS, THE 'OPERATE' TIME BEGINS AT ONE OF THE PULSES OUT OF UL1.

5.16.6 - INTERLOCK WITH NOISE OVERLOAD, END OF SWEEP, ON-OFF, AND EXTERNAL ANALYZER RESET COMMAND: SWEEP-HOLD.

AN 'OPERATE' MODE IS INTERRUPTED, THE ANALYZER THROWN INTO 'RESET' AND THE SWEEP THROWN INTO HOLD BY:

GROUNDING PIN 'X' DUE TO A NOISE OVERLOAD.

GROUNDING PIN 'Z' FROM REMOTE POINT.

GROUNDING CR11 DUE TO END-OF-SWEEP AT PIN 'K', OR OFF ON PIN 'S'.

IF THE ANALYZER IS IN 'HOLD', IT WILL NOT GO INTO 'RESET' UNTIL THE FULL 'HOLD' TIME IS COMPLETED.

UL7B PUTS THE SWEEP INTO 'HOLD', AND KEEPS IT THERE AS LONG AS ANY OF THE ABOVE INPUTS REMAIN AT GROUND. IT COMES OUT OF SWEEP HOLD AS SOON AS 'RESET' IS OVER AND A NEW CYCLE OF ANALYSIS STARTS.

5.16.7 - MISCELLANEOUS

1) ON-OFF

AN 'OFF' COMMAND AT PIN 'S'.

COMMAND 'RESET DC/FREQUENCY CONVERTER' - THRU UL5C, CR14, UL5F. IT ALSO COMMANDS UL7B INTO 'SWEEP-HOLD', AND PREVENTS UL8D FROM PASSING UL1 PULSES.

2) STOP (END-OF-SWEEP) AT PIN 'K' PERFORMS ALL OF THE FUNCTIONS AS 'OFF'.

3) REMOTE RESET - PIN 'W' TO J102-18

-15 VOLTS ON PIN 'W' ALLOWS THE ANALYZER TO COMPLETE THE CYCLE OF ANALYSIS AND GO THRU 'HOLD' TO 'RESET'. THE ACTION OF UL8D 'AND GATE' IS TO PREVENT THE PULSES FROM UL1 TAKING THE TIMING OUT OF 'RESET' AS LONG AS PIN 'W' IS AT -15 VOLTS.

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5.16.8 - ADJUSTMENTS & TEST POINTS

NO ADJUSTMENTS

J0 - GROUND

J1 - 4 PULSES/CYCLE OUT OF UL1 - USE ONLY IN FREQUENCY RANGE 1, 2, 3 & 4.

J2 - PULSES OUT OF DIVIDER UL3.

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5.18 - MULTIPLE REGULATOR

REFERENCE: DRAWING NO. C103376-5

5.18.1 - PURPOSE

THE MULTIPLE REGULATOR HAS TWO RECTIFIED, FILTERED PLUS AND MINUS INPUTS FROM THE POWER SUPPLY.

THE REGULATOR BOARD PROVIDES TWO HIGHLY REGULATED, ISOLATED, LOW NOISE ±15 VOLT SUPPLIES FOR THE 916.

5.18.2 - ±15 VOLT SUPPLY - #1 - A1, Q1, A2, Q2

A PLUS 6 VOLT REFERENCE LEVEL IS ESTABLISHED BY ZENER DIODE CR2 FED BY THE CURRENT SOURCE CR1.

A1 COMPARES THIS REFERENCE THRU R1, R19 WITH A PORTION OF THE OUTPUT AS SET BY POT R8 IN THE CHAIN R7, R8, R9 THRU R3. THE ERROR IS INTEGRATED R2 C1 AND DRIVES Q1 THRU THE SHIFTER CR4 IN SUCH A SENSE AS TO HOLD THE OUTPUT CONSTANT AT +15 VOLTS.

Q1 IS A POWER DARLINGTON PAIR. C7, C11 ASSIST IN FILTERING THE OUTPUT.

AMP 2 COMPARES ITS OWN OUTPUT WITH THE +15 VOLT REGULATOR OUTPUT AS SET BY POT R17 IN THE CHAIN R16, R17, R18. THE ERROR IS AMPLIFIED AND INTEGRATED (R12, C4) TO DRIVE Q2 THRU LEVEL SHIFTING ZENER DIODE CR5. THE OUTPUT AT PIN 'T' IS HELD AT -15 VOLTS OVER LARGE LOAD AND LINE CHANGES.

C13, C12 AIDS IN FILTERING THE OUTPUT. Q2 IS A POWER DARLINGTON PAIR.

A SEPARATE GROUND LINE - PIN 'H' IS USED FOR THIS SUPPLY.

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5.18 - MULTIPLE REGULATOR

5.18.3 - ±15 VOLT SUPPLY - #2 - A3, A4, Q3, Q4

THIS INDEPENDENT ±15 VOLT SUPPY IS IDENTICAL TO 5.18.3. SUBSTITUTE A3 FOR A1; Q3 FOR Q1; A4 FOR A2; Q4 FOR Q2, ETC.

THE RESULT IS A SECOND ±15 VOLT OUTPUT WITH ITS OWN GROUND - PIN 'S'.

5.18.4 - TEST POINTS & ADJUSTMENTS

NOTE: ALWAYS ADJUST PLUS 15 FIRST.
SEE SECTION 6.2 FOR ADJUSTMENT PROCEDURE.

J2	-	+15 VOLTS #1
R8	-	ADJUSTMENT OF +15 VOLTS ON J2
J1	-	-15 VOLTS #1
R17	-	ADJUSTMENT OF -15 VOLTS ON J1
J3	-	+15 VOLTS #2
R30	-	ADJUSTMENT OF +15 VOLTS ON J3
J4	-	-15 VOLTS #2
R40	-	ADJUSTMENT OF -15 VOLTS ON J4

2) PHASE - M2 - S17A IN 'PHASE' -

PHASE IS SCALED ON BOARD #13 TO READ ±1.80 VOLTS. THE DECIMAL POINT FOR 180.0 DEGREES DISPLAY (TO NEAREST 0.1°) IS ALWAYS ENERGIZED.

3) A.R. (DB)- S16C - 'DB RATIO' - M1

AMP CH#1 (DB) - S16B- 'DB1' - M1

AMP CH#2 (DB) - S16A- 'DB2' - M1

ALL THREE INPUTS ARE AT 2.0 VOLTS PER 20 DB. THEY ARE SCALED DOWN 10/1 BY R14, R15 TO DIRECT READ ON M1 WITH THE DECIMAL POINT TO GIVE A DIRECT READING TO THE NEAREST 0.1 DB. THUS, '+20.0' DB FOR AN A.R. OF 10/1.

AMP (DB) IS SCALED FOR ZERO DB = 1.0 VOLT PEAK (OF FUNDAMENTAL). +20.0 ' DB = 10.0 VOLT PEAK: -20.0 DB = 0.10 VOLT PEAK.

4) OFFSET - S16D - M1

THE METER DIRECT READS TO ±10.00 VOLTS. THUS, THE DECIMAL POINT IS MOVED FOR S16D DEPRESSED.

OFFSET IS ONLY READABLE WHEN THE TEST SIGNAL IS 'OFF'. (USE S5).

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5.19 - RIGHT HAND CABLE & FRONT PANEL BOARDS - (DIGITAL READOUTS)

REFERENCE: DRAWING NO. C102992-3

5.19.1 - FUNCTIONS

THE RIGHT HAND CABLE AND FRONT PANEL BOARDS PERFORM THE FOLLOWING FUNCTIONS:

1) THE DIGITAL LOCIC AND SCALING IS PROVIDED TO MAKE THE DIGITAL READOUTS DIRECT READING.

2) DIGITAL CIRCUITRY IS INCLUDED WHICH GENERATES THE DIGITAL LOGIC LEVELS EQUIVALENT TO THE METER READINGS FOR REMOTE READOUT.

EACH OF THESE FUNCTIONS IS DESCRIBED IN DETAIL BELOW:

5.19.2 - DIRECT READING OUTPUTS -

1) FREQUENCY -

UL1 DECODES THE INPUT LOGIC FOR FREQUENCY RANGE ON PINS 5 FR (1 + 2), 6 FR (3 + 4), E (FR ALT) TO DRIVE THE THREE INDICATORS DS11, DS12, DS13 FOR MILLIHERTZ, HERTZ, AND KILOHERTZ; AND TO DRIVE THE DECIMAL POINTS ON M2 THRU Q2, Q4, Q5 AND Q6. THE FOLLOWING 'FREQUENCY' DISPLAY RESULTS.

FR	READING			INDICATOR
1	100	TO	1000	MILLIHERTZ
2	1.00	TO	10.00	HERTZ
3	10.00	TO	100.00	HERTZ
4	100	TO	1000	HERTZ
5	1.00	TO	10.00	KILOHERTZ
6	10.0	TO	100.0	KILOHERTZ

WHEN S17B SELECTS 'FREQUENCY'

THE D.C. VOLTAGE LINEARLY PROPORTIONAL TO FREQUENCY IS 10 VOLT F.S. R14, R13 PROVIDE A 1/10 ATTENUATION TO SCALE TO M2'S 1.000 VOLT RANGE.

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6. - MAINTENANCE & CALIBRATION

6.1 - INTRODUCTION

6.1.1 - GENERAL

EVERY EFFORT HAS BEEN MADE TO BUILD IN STABLE, RELIABLE PERFORMANCE INTO THE MODEL 916.

BEYOND THIS, THERE HAVE BEEN SEVERAL STEPS TAKEN TO MINIMIZE THE NORMAL MAINTENANCE AND CALIBRATION PROCEDURES. THESE INCLUDE.

1) LOCATING ALL OF THE KEY ADJUSTMENTS AND TEST POINTS AT THE FRONT OF THE P.C. BOARDS.

2) IDENTIFYING SEVERAL LEVELS OF CALIBRATION.
NOTE: SEC. 7 FOR A FAST CHECKOUT AND CALIBRATION PROCEDURE.

3) PRESENTING THE CALIBRATION PROCEDURE WITH GREAT DETAIL.

6.1.2 - POLICY

IN ALL OF THE MAINTENANCE WORK THAT MAY ARISE REMEMBER:

1) THE MODEL 916 WILL BE REPAIRED, RECALIBRATED AT BAFCO, AND BE ON ITS WAY BACK TO YOU WITHIN FIVE WORKING DAYS OF ITS RECEIPT.

2) IF YOU IDENTIFY A DEFECTIVE COMPONENT, A REPLACEMENT WILL BE AIR SHIPPED IMMEDIATELY.

3) ALL OF THE P.C. BOARDS CAN BE REPLACED DIRECTLY WITH SPARE ONES. ADDITIONAL CALIBRATION IS UNNECESSARY.

IF QUESTIONS ARISE, CONTACT BAFCO FOR DIRECT ASSISTANCE IN ALL MAINTENANCE AND CALIBRATION WORK.

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6.1.3 - SAFETY PRECAUTIONS -

ONCE THE FRONT PANEL IS OPENED, THE OPERATOR MUST BE CAREFUL OF THE POWER LINES, AS FOLLOWS:

110 VOLT A.C. POWER IS BROUGHT ON THE RIGHT HAND CABLE BOARD (#19) TO THE FRONT PANEL DIGITAL METERS (M1, M2), AND TO THE POWER ON-OFF SWITCH. THEREFORE, EVERY PRECAUTION MUST BE TAKEN WHEN PERFORMING TESTS IN THAT PORTION OF THE MODEL 916.

IF IT IS NECESSARY TO PUT BOARD #19 ON THE EXTENDER BOARD, THE OPERATOR MUST REMOVE THE POWER CORD (TO J20 ON REAR PANEL) BEFORE ATTEMPTING TO REMOVE BOARD #19, AND HE MUST KEEP THE POWER CORD OUT OF J20 (POWER DISCONNECTED) UNTIL THE EXTENDER BOARD AND THE BOARD #19 HAVE BEEN PROPERLY LOCATED.

DURING ALL TESTING WITH BOARD #19 EXTENDED, OR WITH THE METER CONNECTORS AND P.C. BOARDS EXPOSED, THE OPERATOR MUST KEEP HIS HANDS OFF OF THE EXTENDER BOARD, OFF OF THE CABLE BOARD, AND OFF OF THE METERS, THEIR CONNECTORS, AND THEIR P.C. BOARDS. ONLY TEST PROBES SHOULD TOUCH THESE UNITS.

IF THERE ARE ANY QUESTIONS, CHECK DIRECTLY WITH BAFCO, INC.

AN EXCELLENT (AND RECOMMENDED) PROCEDURE, WHEN PUTTING ANY BOARD ON AN EXTENDER, IS TO FIRST, TURN OFF THE POWER; SECOND, REMOVE THE POWER LINE; THIRD, PUT THE BOARD ON THE EXTENDER AND SECURE IT IN ITS FINAL POSITION; FOURTH, RECONNECT POWER LINE AND RETURN ON THE POWER. THEN, PROCEED WITH TESTS. REPEAT EACH STEP ABOVE WHEN RETURNING BOARD INTO INSTRUMENT.

6.1.4 - ORGANIZATION

THE CHECKOUT AND CALIBRATION OF THE MODEL 916 PROCEEDS IN A LOGICAL SEQUENCE AS GIVEN BELOW. THE POWER SUPPLIES MUST BE CHECKED FIRST. THEY CAN BE THE SOURCE OF ALMOST ANY OF THE MALFUNCTIONS, OR OUT-OF-CALIBRATIONS.

SECTION 6.2 COVERS THE POWER SUPPLY CHECKOUT AND CALIBRATION. - BOARD #18.

SECTION 6.3 COVERS THE SIN AND COS REFERENCE SIGNAL GENERATION AND THE OUTPUT TEST SIGNALS - BOARDS #10, #11 AND LEFT FRONT PANEL.

SECTION 6.4 PRESENTS THE MULTIPLIER - INTEGRATORS - BOARDS #7 AND #8.

SECTION 6.5 PRESENTS THE ATTENUATION SYSTEM WITH THE 7 KHZ BOARD.

SECTION 6.6 COVERS THE PHASE AND AMPLITUDE COMPUTERS - BOARDS #13 AND #14.

SECTION 6.7 COVERS THE INPUT PREAMPLIFIER AND INPUT AMPLIFIER - BOARDS #3 AND #4 AND LEFT FRONT PANEL.

SECTION 6.8 COVERS THE AMP DB, AND AMP RATIO DB COMPUTATION - BOARD #12 AND PORTIONS OF BOARDS #3 AND #4.

SECTION 6.9 PRESENTS THE SWEEP SYSTEM - BOARD #2.

SECTION 6.10 COVERS THOSE BOARDS THAT DO NOT HAVE A CALIBRATION BUT WHICH MAY MALFUNCTION.

THESE ARE -

6.10.1 - 'X5' INTEGRATE - BOARD #11
6.10.2 - TIMING - BOARD #16
6.10.3 - DIGITAL READOUT - BOARD #19
6.10.4 - AUTOMATIC GAIN CONTROL - BOARD #5

SECTION 6.11 REVIEWS THE STEPS THAT WERE TAKEN TO MAKE THE 'ANALYSIS CORRECT AT THE HIGH END OF THE HIGH FREQUENCY RANGE.

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6.1.5 - TEST EQUIPMENT

THE FOLLOWING ITEMS OF TEST EQUIPMENT ARE RECOMMENDED. IN ALL CASES THERE ARE OTHER UNITS THAT ARE EQUALLY QUALIFIED. THE ACCURACY SHOULD BE AT LEAST AS GOOD AS THE INDICATED SCALES.

1) DIGITAL VOLTMETER -

HEWLETT PACKARD - 3465A - 4 1/2 DIGIT.

THE KEY PARAMETERS THAT MUST BE MATCHED ARE: D.C. VOLT ACCURACY OF ±.02% OF READING, ±.01% OF RANGE FROM 100 MV TO 100 VOLTS; A.C. VOLT ACCURACY - 100 MV TO 100 VOLT, 40 HZ TO 10 KHZ - ±.15% OF READING, ±.05% OF RANGE.

2) OSCILLOSCOPE -

PHILIPS - PM3234 - 10 MHZ DUAL BEAM STORAGE

THE SLOW SWEEP, STORAGE, AND DUAL BEAM ARE PARTICULARLY USEFUL FOR THE TIMING DISPLAY, INTEGRATION, ETC. AT THE LOWER FREQUENCIES, OR FOR PULSE DISPLAY WHEN THEY OCCUR AT RELATIVELY LONG INTERVALS.

3) COUNTER-TIMER -

HEWLETT - PACKARD MODEL 5304A WITH 5300B MAIN FRAME

THE 5304A HAS THE RANGE OF CAPABILITIES NEEDED FOR FREQUENCY CALIBRATION DOWN TO .01 HZ AND YET MEASURES THE PERIOD OF THE NARROW PULSES IN THE ATTENUATOR WITH SUFFICIENT RESOLUTION.

4) DISTORTION METER -

HEWLETT-PACKARD - MODEL 331A

THERE ISN'T A SPECIAL REQUIREMENT FOR THIS UNIT.

5) PHASE METER -

KROHN-HITE - MODEL 6400

ALL OF THE ADJUSTMENTS CAN BE MADE WITHOUT THIS UNIT. SOME MATTERS ARE SIMPLIFIED WITH IT, ESPECIALLY IN THE HIGH END OF THE 10 KHZ RANGE.

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6.2 - POWER SUPPLIES

REFERENCE: DRAWING NO. C103376 - BOARD #18

6.2.1 - CHECKOUT

ANALYZER - S5 - 'OFF'.

READ THE D.C. VOLTAGE AT J1, J2, J3 AND J4.

J1 AND J4 SHOULD READ -15.00 VOLTS TO WITHIN 10 MV (-15.01 TO -14.99 VOLTS).

J2 AND J3 SHOULD READ +15.00 VOLTS TO WITHIN 10 MV (+15.01 TO +14.99 VOLTS).

READ THE A.C. VOLTAGE (RMS) AT J1, J2, J3 J4. THEY SHOULD BE UNDER 2 MV.

IF THE NOISE LEVEL IS SIGNIFICANTLY GREATER THAN 2 MV, THE SUPPLY MAY BE OUT OF REGULATION. THE NOISE SHOULD BE OBSERVED ON AN OSCILLOSCOPE. LARGE 60 OR 120 HZ NOISE COMPONENTS INDICATE A NEED FOR COMPONENT REPLACEMENT IN THE REGULATOR.

6.2.2 - CALIBRATION

ADJUST +15 VOLT OUTPUTS FIRST:

USE R8 TO MAKE J2 CORRECT (+15.000 VOLTS) WITHIN ±2 MV. USE R30 FOR J3.

THEN, ADJUST -15 VOLT OUTPUTS.

USE R17 FOR J1, AND USE R40 FOR J4. ADJUST -15.000 VOLTS WITHIN ±2 MV.

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6.3 - FREQUENCY - SIN & COS REFERENCE SIGNALS, OUTPUT TEST SIGNAL

REFERENCE: SECTION 4.4

6.3.1 - MALFUNCTION

THE FOLLOWING MALFUNCTIONS MAY OCCUR IN THE REFERENCE AND TEST SIGNAL GENERATION SYSTEM:

1) THE TRIANGLE WAVESHAPE MAY BECOME DISTORTED OR FAIL TO OPERATE, AND THE TOTAL SYSTEM MALFUNCTION.

2) FREQUENCY MAY BE OUT OF CALIBRATION.

3) THE REFERENCE SIGNALS MAY DEVELOP EXCESSIVE DISTORTION.

4) THE OUTPUT TEST SIGNAL MAY MALFUNCTION.

5) THE LOG FREQUENCY OUTPUT MAY LOSE CALIBRATION.

6.3.2 - CHECKOUT

IN THE SAME SEQUENCE AS 6.3.1 -

1) USE S6B TO SELECT TRIANGLE WAVESHAPE, AT 10 VOLT F.S. ON S7A, R3 ABOVE .500, OFFSET ZERO ON S8C. EXAMINE ON D.C. COUPLED OSCILLOSCOPE. EXAMINE IN ALL SIX FREQUENCY RANGES. IF IT IS MALFUNCTIONING, THE PROBLEM IS ON THE D.C./FREQUENCY BOARD #10.

   THE TRIANGLE SHOULD BE UNIFORM IN ± HEIGHT VS. FREQUENCY, AND ITS EDGES SHOULD BE STRAIGHT.

2) MOVE S6 TO S6A. PUT THE TIMER - COUNTER ON THE SQUARE WAVE OUTPUT. CHECK FREQUENCY (OR TIME PER CYCLE) VS. FREQUENCY RANGE SETTING OF S1, AND VS. DCS1. (LIN FREQUENCY ON A1 REAR PANEL). USE DVM TO MEASURE DCS1.

   FREQUENCY SHOULD BE WITHIN ±1% OF VALUE. CALIBRATION IS SET BY THE D.C./FREQUENCY BOARD #10.

3) CHECK SINE WAVE OUTPUT DISTORTION. USE 800 HZ AND 10 VOLT F.S. IF OVER 1% RMS, DISTORTION NEEDS ADJUSTMENT.

CHECK COS WAVE (J11 ON REAR PANEL) DISTORTION. IF OVER 1-1/2% RMS, IT NEEDS ADJUSTMENT.

4) OBSERVE THE REFERENCE SIGNALS COS - ON J11 REAR PANEL.
SIN - J1 OF BOARD #9.
TRIANGLE - J1 OF BOARD #10.
SQUARE - J2 OF BOARD #10.

IF THEY ARE SATISFACTORY ABOVE, BUT HAVE A MALFUNCTION WHEN OBSERVED AT J5A (FRONT PANEL), J5B (REAR PANEL), THEN THE OUTPUT AMPLIFIER IS MALFUNCTIONING.

5) CHECK LOG FREQUENCY (REAR PANEL) FOR '0' VOLTS AT 10 HZ, 2.0 VOLT/DECADE. RESULTS SHOULD BE CORRECT TO WITHIN 10 MV (.1 DB - 1% OF VALUE).

IF NOT, LOG FREQUENCY ON BOARD #9 NEEDS CORRECTION.

NOTE:

IF FREQUENCY ACCURACY AND DISTORTIONS ARE WITHIN SPECIFICATION, DO NOT REDO THE CALIBRATION. BOARDS #9 AND 10 ARE PERFORMING AS REQUIRED.

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6.3.3 - CALIBRATION

6.3.3.1 - FREQUENCY - BOARD #10

USE 10 VOLT SQUARE WAVE ON FRONT PANEL J5 AS SOURCE OF COUNTER/TIMER INPUT.

STEP 1 IS TO CHECK AND SET THE TRIANGLE RMS AMPLITUDE. SET FREQUENCY AT 800 HZ.

USE DVM TO READ RMS VALUE AT J1 TO J0. IT SHOULD READ 5.380 VOLTS RMS WITHIN ±5 MV.

IF IT IS OUTSIDE OF THIS RANGE, PUT BOARD #10 ON AN EXTENDER. USE R14 TO ADJUST TRIANGLE AMPLITUDE.

STEP 2 IS TO CHECK AND ADJUST THE D.C. LEVEL. IT SHOULD BE WITHIN ±5 MV OF ZERO. READ ON DVM. USE R20 TO MAKE D.C. CONTENT OF TRIANGLE = ZERO (WITHIN ±2 MV).

STEP 3 IS TO CHECK FREQUENCY AND ADJUST.

USE SQUARE WAVE 10 VOLT OUTPUT TO CHECK FREQUENCY OR TIME PER CYCLE.

CHECK .8 HZ AND ADJUST USING R50.

CHECK OTHER FREQUENCIES FROM .1 TO 10 HZ. SELECT SETTING OF R50 WHICH BEST BRINGS BOTH RANGES WITHIN 1% OF VALUE.

IF LOW END OF FREQUENCY RANGES IS OUT OF SPECIFICATION, A1A OR A1B ON BOARD #10 HAS AN OFFSET. THEIR IS PROVISION FOR A TRIM OFFSET BY A RESISTOR FROM COMMON OF R45, R46 (S) TO THE '+' OR '-' INPUT OF A1A (1^{-}, 1^{+}), AND OF A1B (2^{-}M 2^{+}). THIS MODIFICATION IS SELDOM NECESSARY. USE DCS1 = +10.0 VOLTS; MEASURE A1 OUTPUT, A2 OUTPUT: REDUCE DCS1 TO +1.00 VOLTS. MEASURE A1 OUTPUT, A2 OUTPUT. THEY SHOULD BE EXACTLY 0.1 OF FIRST MEASUREMENT. CHANGE OFFSET RESISTORS AS NEEDED TO MAKE '10%' OUTPUT = 10% OF FULL SCALE OUTPUT.

READJUST R50, R51, R52.

MOVE FREQUENCY TO 800 HZ. ADJUST FREQUENCY USING R51 TO BE WITHIN 1% OF VALUE. CHECK FROM 10 HZ TO 100 HZ. USE R51 IN POSITION THAT BRINGS ALL VALUES WITHIN 1% OF VALUE.

MOVE FREQUENCY TO 8000 HZ. ADJUST FREQUENCY USING R52 TO BE WITHIN 1% OF VALUE.

CHANGE FREQUENCY TO 95,000 HZ. USE C11 (ON BOARD - USE EXTENDER) TO MAKE FREQUENCY CORRECT.

CHECK FREQUENCY FROM 1000 HZ TO 100,000 HZ. SELECT BEST VALUE OF R52 TO HOLD ENTIRE RANGE WITHIN SPECIFICATION.

THIS COMPLETES THE FREQUENCY CALIBRATION.

6.3.3.2 - DISTORTION

SIN -

THE MEASUREMENT OF RMS DISTORTION REQUIRES SOME OPERATOR SKILL IF ONE OF THE MANUAL DISTORTION METERS IS USED.

IT IS RECOMMENDED THAT 800 HZ BE USED FOR DISTORTION CHECK AND ADJUST.

IF THE DISTORTION OF THE SINE WAVE (AT 10 VOLT OUTPUT ON FRONT PANEL OR J1 OF BOARD #9) EXCEEDS 1% RMS, THE FOLLOWING STEPS WILL IMPROVE IT.

FIRST - CHECK THAT THE TRIANGLE WAVE FORM ON J1 OF BOARD #10 IS 5.381 VOLTS RMS ±5 MV. IF NOT, GO BACK TO FREQUENCY ADJUSTMENT AND REDO IT.

SECOND - R4 ON BOARD #10 WILL USUALLY BE THE KEY ADJUSTMENT. IT BALANCES THE TRIANGLE (SAME SLOPE GOING PLUS OR MINUS).

THIRD - IF THESE TWO DO NOT SUFFICE, CHECK D.C. LEVEL OF TRIANGLE. IF IT IS MORE THAN ±5 MV, USE R20 ON BOARD #10 TO ADJUST IT.

NORMALLY, THESE THREE ITEMS WILL RESULT IN A DISTORTION WELL UNDER 1% RMS (TO 1/2% RMS).

FINALLY, USE R65 ON BOARD #9 TO REDUCE D.C. LEVEL OF SINE WAVE TO WITHIN ±5 MV.

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6.4 - DUAL MULTIPLIER - INTEGRATOR

REFERENCE: BOARDS #7 & #8
DRAWING NO. C102973
THEORY - SECTION 4.5.2

6.4.1 - MALFUNCTION - MULTIPLIERS - CHECK FOR MALFUNCTION -

THE MULTIPLIER CAN BE CHECKED BY OBSERVING ITS OUTPUT ON AN OSCILLOSCOPE AND MEASURING IT WITH A DVM. THERE ARE THREE CHECKS THAT RAPIDLY SHOW IF A MALFUNCTION HAS OCCURRED.

1) WITH 'AGC OUT' (REAR PANEL, A1, S20), AND THE INPUTS SHORTED, AND THE ANALYZER OPERATING AT 800 HZ; THE D.C. OUTPUT AT J1 AND J4 SHOULD BE NEAR ZERO VOLTS (WITHIN ±5 MV) AND THE ZERO ADJUSTMENT (R12, R36) SHOULD BE ABLE TO BRING THE D.C. OUTPUT TO ZERO.

2) WITH 10 VOLTS RETURN SIGNAL, THE MULTIPLIER SHOULD SHOW A SECOND HARMONIC OUTPUT. FOR EXAMPLE, WITH 800 HZ INPUT, THE J4 OUTPUT WILL BE A 1600 HZ SIGNAL WITH ABOUT 2.5 VOLTS OF D.C. (RESULT OF SIN X SIN), AND THE J1 OUTPUT WILL BE A 1600 HZ SIGNAL WITH NEAR ZERO VOLTS OUTPUT (RESULT OF SIN X COS MULTIPLICATION).

   A MULTIPLIER MALFUNCTION WILL SHOW ITSELF AS A BADLY DISTORTED OUTPUT, OR A BADLY INCORRECT D.C. LEVEL.

3) USE COS TEST SIGNAL (10 VOLT) AS RETURN SIGNAL AND AGAIN OBSERVE MULTIPLIER OUTPUTS. J4 WILL BE NEAR ZERO VOLTS. J1 WILL BE NEAR 2.5 VOLTS.

   USE COMPARISON OF BOARD #7 AND #8 OUTPUTS TO FURTHER ASSIST IN DETERMINING THE MALFUNCTIONING MULTIPLIER.

   IT IS RECOMMENDED THAT YOU RETURN DEFECTIVE MULTIPLIER-INTEGRATOR BOARD TO BAFCO FOR MULTIPLIER REPLACEMENT.

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6.5 - 7 KHZ - BOARD #15

REFERENCE: DRAWING NO. C103046

6.5.1 - MALFUNCTION

THE 7 KHZ BOARD IS A BASIC PART OF THE PHASE AND AMPLITUDE COMPUTER OPERATION, AND IT HAS THE ENTIRE ATTENUATION CONTROL SYSTEM.

THUS, A MALFUNCTION ON THIS BOARD MAY ONLY SLOW UP IN ONE OR BOTH PHASE AND AMP COMPUTERS, OR IN THE ATTENUATION CONTROL, OR IN ALL THREE.

OBSERVE J1, (OF BOARD #15) ON THE OSCILLOSCOPE. IT SHOULD BE A TRIANGULAR WAVEFORM AT 7 KHZ OF ±7.5 VOLTS, 4.21 VOLT RMS.

IF THIS WAVEFORM IS MISSING, THE BOARD IS MALFUNCTIONING AND THE 7 KHZ OSCILLATOR A1, A2 MUST BE TROUBLE-SHOT AND THE DEFECTIVE COMPONENT REPLACED.

OBSERVE J2 (BOARD #15) IN ONE OF THE FOUR LOW FREQUENCY RANGES. IT SHOULD BE A SQUARE WAVE AT 7 KHZ, WHOSE ON-TIME (AT GROUND) INCREASES AS DCS1 (FREQUENCY) DECREASES FROM 100% TO 10% OF FULL RANGE.

IF THIS WAVEFORM IS NOT PRESENT, THE ATTENUATOR CIRCUIT IS NOT FUNCTIONING.

TO CHECK IF PHASE AND AMPLITUDE PORTION IS WORKING (NO ADJUSTMENTS), PUT BOARD #15 ON AN EXTENDER.

THE CH#1 INPUT SQUARE WAVE IS AN INPUT DURING A PORTION OF THE OPERATE, AND ALL OF THE 'HOLD' PORTION OF TIMING SEQUENCE; PIN 'M' HAS A 7 KHZ SQUARE WAVE (0 TO +10 VOLTS). THIS SHOULD RESULT IN A -15 TO 0 SQUARE WAVE AT PIN 'Y'. IF NOT, CHECK PIN 'L'. IF SQUARE WAVE AT 'L', REPLACE UL3. IF NO SQUARE WAVE AT 'L', REPLACE UL1 AND RECHECK.

SIMILARLY, FOR CH#2, PIN 'K' TO PIN 'V', AND PIN 'B'.

THEN CHECK PIN 'A'. IT SHOULD BE A BALANCED SQUARE WAVE WHEN PHASE = 0°. IF NOT PRESENT, CHECK BACK AND MAKE DECISIONS FOR NEED TO REPLACE UL1, UL3, OR UL2.

NOTE UL2 OUTPUTS ARE SHORT DURATION PULSES AT PLUS TO ZERO EDGE OF PIN 'M' AND PIN 'K' INPUT SQUARE WAVES.

6.5.2 - CALIBRATION

CHECK FREQUENCY AT J1. IT SHOULD BE 7030 HZ. USE R19 TO MAKE IT 7030 HZ.

WITH DCS1 = 1.000 VOLTS AND THE 916 IN ONE OF THE FIRST FOUR FREQUENCY RANGES, USE COUNTER-TIMER TO READ 'ON' TIME AT J2. IT SHOULD BE 128.8 MICROSECONDS. IF NOT, USE R51 TO ADJUST IT.

CHANGE DCS1 TO 10.000 VOLTS. THE 'ON' TIME SHOULD BE 12.9 MICROSECONDS. IF NOT, USE R18 TO ADJUST TO JUST UNDER 12.9.

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6.6 - PHASE & AMP COMPUTERS - BOARDS #13 & #14

REFERENCE: DRAWING NO. C103401-1,2 & SECTION 4.7.1

6.6.1 - MALFUNCTION

A FAILURE IN ONE OF THESE BOARDS WILL SHOW ITSELF AS TOTALLY ERRONEOUS PHASE, AMP CH#1 DB, OR AMP CH#2 DB RESULTS OR SOME COMBINATION OF THESE. IT IS BEST DETECTED BY OPERATING THE MODEL 916 WITH KNOWN INPUTS, AND WITH AUTOMATIC GAIN CONTROL 'OUT' (SW20 ON A1 OF REAR PANEL).

IF THE MULTIPLIERS, AND INTEGRATORS WORK PROPERLY, BUT PHASE, AND OR AMPLITUDE DOES NOT, THEN THESE BOARDS MUST BE TROUBLE SHOT, AS PRESENTED IN THE FOLLOWING SECTION.

6.6.2 - CHECK FOR MALFUNCTION

SET THE AUTOMATIC GAIN CONTROL 'OFF'. BOARD #13, AND THEN BOARD #14 ON AN EXTENDER.

OPERATE THE ANALYZER AT 800 HZ, 10 VOLTS TO CH#1 AND CH#2. USE 'X5 IN'. OBSERVE THE TEST PIN AT THE OUTPUT OF A1.

ITS OUTPUT WILL GROW AS THE INTEGRATOR OUTPUT INCREASES. AT 7 KHZ, A1 OUTPUT IS A SQUARE WAVE PASSED THRU A FILTER HAVING A SERIES OF EXPONENTIALS. ONE END NEAR GROUND, AND THE OTHER, AT AN AMPLITUDE PROPORTIONAL TO THE INPUT. THE WAVEFORM COLLAPSES TO ZERO DURING THE RESET MODE.

IF THIS WAVEFORM IS NOT PRESENT, A1, Q1, Q2, Q3 OR Q4 IS DEFECTIVE. REPLACE AND CHECK AGAIN.

THEN OBSERVE OUTPUT OF A2 AT TEST PIN (2). IT WILL BE A SINE WAVE AT 7 KHZ AROUND ZERO, WHOSE AMPLITUDE INCREASES AS THE INTEGRATOR OUTPUTS INCREASE. THE SINE WAVE COLLAPSES AT THE END OF THE 'HOLD' PERIOD AND REMAINS AT ZERO DURING 'RESET'.

IF THIS WAVEFORM IS NOT PRESENT, A2 IS DEFECTIVE. REPLACE IT AND RECHECK.

THEN OBSERVE OUTPUT OF A3 AT TEST PIN (3). IT IS A SQUARED VERSION OF A2 OUTPUT, AT ± .4 VOLTS. IT IS NEAR GROUND DURING 'RESET' MODE.

IF THIS WAVEFORM IS NOT PRESENT, REPLACE A3.

THEN OBSERVE A6 OUTPUT AT PIN 'W' (OR AT R69). IT IS A SQUARE WAVE FROM +.7 VOLTS TO +10 VOLTS AT 7 KHZ. IT IS +10 VOLTS DURING 'RESET'.

IF THIS WAVEFORM IS NOT PRESENT, REPLACE A6, Q11.

OBSERVE AMPLITUDE SIGNAL AT COMMON OF R40, R41. IT IS HALF WAVE RECTIFIED (MINUS PORTION) OF A2 OUTPUT (ATTENUATED BY 2/1).

IF THIS WAVEFORM IS NOT PRESENT, CHANGE Q7. (REMEMBER 7 KHZ BOARD WAS CHECKED FIRST. SQUARE WAVE AT PIN 'D' IS ASSUMED TO BE CORRECT).

VARY TEST SIGNAL AMPLITUDE AND OBSERVE A4 OUTPUT STEP FROM +5.0 VOLT F.S. LINEARLY DOWN AS INPUT IS REDUCED (PROPORTIONAL). IF NOT, CHANGE Q9 FIRST. IF STILL NOT, CHANGE A4.

THE PHASE CHECKOUT STARTS AT BOARD #14. (AGAIN IT IS ASSUMED 7 KHZ BOARD HAS BEEN CHECKED). PIN 'C' OF BOARD #14 IS A SQUARE WAVE, '0' TO '-15' VOLTS AT 7 KHZ. AT 0° PHASE, IT IS HALF 'ON' AND HALF 'OFF'.

COMMON OF R64, R51 IS A SQUARE WAVE, GROUND TO NEAR +7.5 VOLTS AT 7 KHZ. IF NOT, CHANGE Q8.

A5 OUTPUT GOES TO NEAR GROUND DURING 'HOLD'. IF NOT, REPLACE A5.

ON BOARD #13, A5 OUTPUT READS THE PHASE. IT REMAINS NEAR ZERO. CHANGE THE PHASE, USE 90° TEST SIGNAL ON ONE CHANNEL. A5 OUTPUT MOVES TO NEAR 90° VALUE, AND REMAINS THERE. IF NOT, REPLACE Q9 FIRST. THEN, IF NOT CORRECTED, REPLACE A5.

6.6.3 - CALIBRATION

1) NULL OF MODULATION PULSES
BOARDS #13 & #14 IN TURN

PUT S5 IN 'OFF'. THIS SETS INPUT (INTEGRATOR OUTPUTS) TO ZERO D.C. LEVEL.

OBSERVE THE A.C. OUTPUT OF A2 ON AN OSCILLOSCOPE. WORK SENSITIVITY DOWN TO 10 MV/CM.

USE R6 AND R12 TO NULL THE A.C. CONTENT OF A2 OUTPUT AT 7 KHZ. IT SHOULD BE POSSIBLE TO REDUCE IT TO BELOW 5 MV.

2) PROCEED WITH ZERO ADJUSTMENT OF R55 AS DESCRIBED IN FAST CHECKOUT, SEC. 7.3, STEP 3.

3) OPERATE THE 916 AT 80. HZ, 'X5 IN', AND 10 VOLT OUTPUT CONNECTED AS AN INPUT TO BOTH CHANNELS.

SET PHASE TO ZERO '00.0' ON THE METER USING R50 OF BOARD #13.

USE A '+' INPUT ON ONE CHANNEL, AND A '-' INPUT ON THE OTHER CHANNEL. ADJUST PHASE SPAN R47 FOR 180.0 DEGREE READOUT (1.800 VOLTS AT PHASE READOUT, J2).

4) CHANGE INPUT TO COSINE FROM J11 OF REAR PANEL. SET AMPLITUDE SPAN AT +5.00 VOLTS FOR FULL SCALE INPUT USING 'R44' AND TEST POINT J1. PERFORM ON BOTH CHANNELS.

5) REPEAT (4) FOR SINE INPUT (TEST SIGNAL OUTPUT).

CHECK FOR +5.00 VOLTS AT J1 ON EACH BOARD. ADJUST 'R4' TO MAKE SIN AMPLITUDE GAIN = COS AMPLITUDE GAIN.

6) USING SIN INPUT REPEAT TEST CONDITION OF (4) ABOVE. REDUCE TEST SIGNAL TO PRECISELY 10% OF FULL SCALE. USE A.C. DVM TO CHECK RATIO 7.07 VOLT RMS TO .707 RMS.

TRIM AMPLITUDE OUTPUT J1 USING R54 TO MAKE AMPLITUDE OUTPUT = +0.500 VOLT.

REDO ON 100% TO 10.0% INPUT UNTIL 5.00, AND .500 VOLTS ARE THE NET AMPLITUDE OUTPUT.

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6.6.4 - SUMMARY

THE STABILITY OF THE PHASE AND AMPLITUDE COMPUTERS ARE SUCH THAT THE FAST CHECKOUT PROCEDURE SHOULD BE SUFFICIENT.

THE COMPLETE PROCEDURE IS ONLY JUSTIFIED WHEN THE FAST PROCEDURE DOES NOT BRING THE MODEL 916 INTO SPECIFIED PERFORMANCE.

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6.7 - INPUT AMPLIFIER - BOARDS #3 & #4

REFERENCE: DRAWING NO. C103110

6.7.1 - MALFUNCTION

THE MOST PROBABLE MALFUNCTION OF THE INPUT AMPLIFIER IS AN AMPLIFIER FAILURE OR A FET FAILURE.

AMPLIFIER FAILURE WILL SHOW AS A HARD OVER ±12 VOLTS D.C. AT J1. TRACE BACK AND FIND THE DEFECTIVE AMPLIFIER.

FET FAILURE WILL SHOW AS A PROBLEM OPERATING AT CERTAIN GAIN LEVELS. LOWER THE INPUT SIGNAL AND TRY TO IDENTIFY THE DEFECTIVE FET. THE ADDED FET ASSOCIATED WITH EACH GAIN SETTING IS Q1 WITH 'X2', Q2 WITH 'X4', Q3 WITH 'X8', Q5 WITH X16, Q4 WITH 'X256'.

6.7.2 - CHECK AND CALIBRATION

THE ONLY CHECKS ARE THE ZERO OFFSET OF THE HIGH PASS FILTER, AND THE SPAN OF THE GAIN TO DB CONVERTER.

AT J1 THE D.C. OFFSET SHOULD BE UNDER 50 MV. WITH 10 VOLT RETURN SIGNAL, CHECK D.C. LEVEL AT J1 FOR .1K AND 1K FREQUENCY RANGES. IF NECESSARY, ADJUST R18 TO MINIMIZE THE D.C. OFFSET (BEST COMPROMISE FOR BOTH FREQUENCY RANGES).

6.7.3 - OTHER

1) DB VS. GAIN - SEE SEC. 6.8

WITH 10 VOLT RETURN SIGNAL, CHECK D.C. LEVEL AT J2. IT WILL BE WITHIN ±5 MV OF ZERO VOLTS, (OR USE S20 ON A1 REAR PANEL FOR AUTOMATIC GAIN CONTROL 'OUT'). IF IT NEEDS ADJUSTMENT, ADD SELECTED 'R' FROM (1) TO (2) OR (3).

DEPRESS S10 - 'PRESET GAIN' - ON FRONT PANEL. J2 SHOULD READ +4.80 VOLTS WITHIN ±5 MV. USE R60 TO ADJUST.

2) HIGH FREQUENCY

R10 C7, AND R25 C19 HAVE BEEN SELECTED TO CORRECT THE GAIN AND PHASE SHIFT IN THE HIGH FREQUENCY RANGE FOR THE X16 VOLTS/VOLT AND HIGH SENSITIVITIES. SECTION 6.11 COVERS THIS MATTER.

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916XH

6.8 - AMPLITUDE IN DB, AMPLITUDE RATIO DB - BOARD #12 AND PORTIONS OF BOARDS #3 & #4

REFERENCE: FIG. 4.7-2
DRAWINGS NOS. C103395 & C103110

6.8.1 - MALFUNCTION

A MALFUNCTION IN THESE CALCULATIONS WILL SHOW AS INCORRECT DB READOUTS EVEN THOUGH THE ANALYZER IS FUNCTIONING CORRECTLY IN ALL OTHER RESPECTS.

6.8.2 - TROUBLESHOOTING

PUT IN TO BOTH CHANNELS 10.0 VOLT SIGNAL FROM THE ANALYZER OUTPUT AT 80 HZ. READ DB CH#1, DB CH#2, DB RATIO. THEY SHOULD READ +20.0 DB, +20.0 DB, 0.00 DB. IF ONE OR MORE ARE OUT BY A FEW TENTHS OF A DB, IT IS A CALIBRATION PROBLEM AND CAN BE CORRECTED BY THE PROCEDURES OF SECTION 6.8.3. IF ONE OR MORE ARE OFF BY SEVERAL TO TENS OF DB, THE DB COMPUTING SYSTEM MUST BE TROUBLESHOT FOR A MALFUNCTION.

BEFORE PROCEEDING, BE CERTAIN THAT THERE IS NO OVERLOAD OR UNDERLOAD INDICATION. EITHER OF THESE WOULD SHOW THAT THE PROBLEM IS MORE LIKELY IN THE AUTOMATIC GAIN CONTROL SYSTEM. ALSO, CHECK AMPLITUDE CH#1 AND CH#2 AT THE PHASE AND AMPLITUDE BOARD. IT SHOULD READ +5.00 VOLTS AT J1 OF BOARDS #13 AND #14. IF SIGNIFICANTLY OFF OF +5.00 VOLTS, THERE IS FIRST A PROBLEM IN THE REMAINDER OF THE ANALYZER.

STEP 1

PUT AUTOMATIC GAIN CONTROL 'OFF', J102-12 TO GROUND OR HOLD SW20 IN 'OFF' POSITION.

CHECK D.C. VOLTAGE AT J2 OF BOARDS #3 AND #4. IT SHOULD READ ZERO (WITHIN 10 MV). IF IT IS SIGNIFICANTLY OFF, A5, Q10, Q11, Q12, Q13 OF THE RESPECTIVE BOARD #3 OR #4 MUST BE CHECKED AND REPLACED AS FOUND NECESSARY.

STEP 2

WITH 'AGC OUT', AND ANALYZER AT 80.0 HZ, REDUCE INPUT TEST SIGNAL TO 1.0 VOLT PEAK. PUT BOARD #12 ON AN EXTENDER. CHECK ANODE OF CR13, CR12, CR11, CR10. ALL SHOULD BE AT APPROXIMATELY -.44 VOLTS. THE ONE (OR MORE) THAT IS FAR REMOVED FROM THIS VALUE INDICATES A DEFECTIVE AMPLIFIER, OR TEMPERATURE STABILIZED TRANSISTOR. REPLACE AND RECHECK AS INDICATED. IF ALL FOUR ARE CORRECT, THE MALFUNCTION IS ASSOCIATED WITH UL3A OR B.

STEP 3

IF ONLY DB RATIO IS INCORRECT, REPLACE A5.

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STEP 2

WITH 'AGC OUT', AND ANALYZER AT 80.0 HZ, REDUCE INPUT TEST SIGNAL TO 1.0 VOLT PEAK. PUT BOARD #12 ON AN EXTENDER. CHECK ANODE OF CR13, CR12, CR11, CR10. ALL SHOULD BE AT APPROXIMATELY -.44 VOLTS. THE ONE (OR MORE) THAT IS FAR REMOVED FROM THIS VALUE INDICATES A DEFECTIVE AMPLIFIER, OR TEMPERATURE STABILIZED TRANSISTOR. REPLACE AND RECHECK AS INDICATED. IF ALL FOUR ARE CORRECT, THE MALFUNCTION IS ASSOCIATED WITH UL3A OR B.

STEP 3

IF ONLY DB RATIO IS INCORRECT, REPLACE A5.

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6.8.3 - CALIBRATION

THERE ARE THREE STEPS IN DB CALIBRATION:

1) REFINE THE DB-GAIN OUTPUT OF THE INPUT AMPLIFIER.

DEPRESS THE 'PRESET GAIN' (S10) ON FRONT PANEL. USE DVM TO MEASURE D.C. LEVEL AT J2 OF BOARDS #3 AND #4. IT SHOULD READ 4.800 VOLTS ±5 MV. USE R60 TO CORRECT IF NECESSARY.

2) SET 916 TO 800 HZ, 100% FULL SCALE OUTPUT TO BOTH INPUTS AND WITH 'AGC OUT'. CHECK AMPLITUDE AT PHASE AND AMPLITUDE BOARDS #13 AND #14, J1. IT SHOULD READ 5.00 VOLTS. ADJUST TEST SIGNAL UNTIL RESULT IS WITHIN 10 MV. (DO ONE CHANNEL AT A TIME - BOARD #13 - CH#1; BOARD #14 - CH#2).

ON BOARD #12, ADJUST R37 FOR CH#2 DB OUTPUT AT J2 = +2.00 VOLTS. THEN ADJUST R28 FOR CH#1 DB OUTPUT AT J1 = +2.00 VOLTS.

3) REPEAT SETUP OF STEP 2, WITH TEST SIGNAL = 1.00 VOLTS PEAK. AMPLITUDE AT J1 OF BOARDS #13 AND #14 SHOULD BE .500 VOLTS WITHIN 2. MV. (USE ONE CHANNEL AT A TIME FOR MOST PRECISE WORK).

ON BOARD #12, ADJUST R59 FOR +0.000 VOLTS AT J1, WITHIN ±5 MV. ADJUST R60 FOR +0.000 VOLTS AT J2 WITHIN ±5 MV.

THIS COMPLETES THE CALIBRATION OF THE AMPLITUDE DB AND AMPLITUDE RATIO DB BOARD. THE STABILITY OF THESE PARTS ARE SUCH THAT ONLY THE 20 DB ADJUSTMENT IS BROUGHT TO THE FRONT OF THE P.C. BOARD. A CAREFUL CHECK AGAINST PRECISELY SET AMPLITUDE INPUT FROM THE PHASE AND AMPLITUDE BOARDS WILL USUALLY SHOW THAT FURTHER ADJUSTMENT IS UNNECESSARY.

REPEAT ADJUSTMENTS WILL NORMALLY BE LIMITED TO R28 AND R37.

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6.9 - SWEEP

REFERENCE: SECTION 4.4.5
DRAWING NO. C102708 - BOARD #2

6.9.1 - MALFUNCTION - CHECK

THE SWEEP SYSTEM MAY EXPERIENCE THE FOLLOWING MALFUNCTIONS:

1) IT FAILS TO SWEEP WHEN PUT INTO SWEEP. CHECK A1 BOARD #2, AND ITS 'RESET' FET-Q4. IT IS NOT COMING OUT OF 'RESET'.

2) IT FAILS TO 'HOLD' WHEN PUT INTO 'HOLD'. CHECK Q3 ON BOARD #2. IT IS NOT TURNING OFF.

3) IT FAILS TO CHANGE FREQUENCY RANGE WHEN IT REACHES 100% OF START FREQUENCY RANGE ON BOARD #2. CHECK Q11 OFF; CHECK J2 AT -15 VOLTS. IF NOT, A3 IS DEFECTIVE. CHECK COMMON R63, CR25, CR28, AT -15 VOLTS. IF AT GROUND, FIND CAUSE AND CORRECT.

   IF ALL OF ABOVE ARE CORRECT, REPLACE UL3 AND TRY AGAIN. THEN REPLACE UL1 AND TRY AGAIN. THE ONE SHOT SHOULD FIRE WHEN THE INPUT GOES FROM GROUND TO -15 VOLTS. THE UP/DOWN COUNTER SHOULD ADVANCE ONE COUNT WHEN UL3 FIRES.

4) FINALLY, FREQUENCY RANGE MAY NOT SWITCH CORRECTLY FROM 100% OF ONE RANGE TO 10% OF SUCCEEDING RANGE. THIS IS A CALIBRATION GIVEN BELOW.

6.9.2 - CALIBRATION OF FREQUENCY RANGE SWITCHING POINTS

SET THE START AND STOP FREQUENCY RANGES APART BY AT LEAST ONE FREQUENCY RANGE.

HOLD SW21 IN 'CAL', OR PUT -15 VOLTS TO J102-13, AND PUT GROUND TO J102-15.

SWEEP IN RESET. FREQUENCY IS CONTROLLED BY R42 ON FRONT OF BOARD #2. ADJUST R42 TO EXACTLY 10% OF FULL SCALE (LIN FREQUENCY = 1.00 VOLT - AT J1 OF BOARD #2).

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RAPIDLY SWEEP TO HIGH END OF FREQUENCY RANGE. FREQUENCY SHOULD STOP AT FULL SCALE (LIN FREQUENCY = 10.00 VOLT AT J1 OF BOARD #2). ADJUST R52 ON FRONT OF BOARD #2, REDO SWEEP UNTIL STOP OCCURS AT 10.00 VOLT ON J1 OF BOARD #2.

THIS COMPLETES SWEEP SWITCHING POINT CALIBRATION.

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6.10 - BOARDS (AND SYSTEMS) WITHOUT CALIBRATION

6.10.1 - 'X5' INTEGRATE BOARD #11

REFERENCE: DRAWING NO. C103306

A MALFUNCTION ON THIS BOARD WILL SHOW ITSELF AS DESCRIBED BELOW AND SHOULD BE FOLLOWED BY THE CORRECTIVE ACTION GIVEN:

1) UL1, UL4

FAILURE OF THE OVERLOAD LIGHT TO FUNCTION - CHECK PIN 'C', AND PIN '5'. IF AT -15 VOLTS AND OVERLOAD NOT 'ON', RESPECTIVE LIGHT IS DEFECTIVE (PRODUCE OVERLOAD BY DEPRESSING PRESET GAIN WITH HIGH LEVEL FEEDBACK SIGNAL).

IF PINS 'C' AND OR '5' FAIL TO GO TO -15 VOLTS IN RESPONSE TO OVERLOAD, REPLACE UL1.

CHECK SHORT 'RESET' PULSE AT PIN 'B', FOLLOWING RESET TO GROUND AT PIN '1'. REPLACE UL4 IF NOT PRESENT.

2) UL5, UL6

IF SOME FREQUENCY RANGES DO NOT FUNCTION CORRECTLY, CHECK LOGIC LEVELS AT PINS '13', '11' '22'. IF INCORRECT, CHANGE UL5 AND OR UL6.

3) UL7, UL8

WITH THE BOARD #11 ON AN EXTENDER, USE AN OSCILLOSCOPE TO CHECK WAVESHAPES AT (1), (2), (3).

THESE SHOULD BE -

(1) 220 HZ - 1/2 ON, 1/2 OFF.

(2) 1757 HZ.

(3) 176 HZ - 1/10 ON (GROUND), 9/10 OFF (-15).

IF (1) OR (2) ARE MALFUNCTIONING, CHANGE UL8.

IF (3) IS MALFUNCTIONING, CHANGE UL7.

4) UL2, UL3

THE CORRECT OPERATION OF THE LOGIC IN THESE INTEGRATED CIRCUITS WILL SHOW ON J1 OF BOARD #11. IN FR3, 4, 5, AND 6, THE READ-HOLD COMMAND WILL REPRODUCE AT J1.

IN (FR2)$\cdot\overline{(X5)}$, THE READ-HOLD IS UNCHANGED.

IN (FR2)$\cdot$(X5), A 1/2 ON, 1/2 OFF SQUARE WAVE AT 220 HZ MODULATES THE OPERATE TIME.

IN (FR1)$\cdot\overline{(X5)}$, A 1/10 ON, 9/10 OFF SQUARE WAVE AT 176 HZ MODULATES THE OPERATE TIME.

IN (FR1)$\cdot$(X5), A 1/20 ON, 19/20 OFF SQUARE WAVE AT 88 HZ MODULATES THE OPERATE TIME.

IF ONE OF THESE ARE IN ERROR, CHANGE UL2 AND UL3.

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6.10.2 - TIMING BOARD #16

REFERENCE: DRAWING NO. C103314-1
SEC. 5.16, SEC. 4.6, FIG. 4.6-1

A MALFUNCTION IN THE TIMING SYSTEM SHOWS ITSELF AS: THE 'X5' INTEGRATE GIVES A DIFFERENT RESULT FROM 'X5' INT' 'OUT'; OR THE RESULTS VARY MARKEDLY FROM TEST RUN TO TEST RUN; OR THE TIMING SYSTEM HANGS UP IN RESET OR HOLD, ETC. ANY ONE OF THESE ARE THE RESULT OF A FAILURE OF ONE OF THE INTEGRATED CIRCUITS. (THERE IS NO CALIBRATION ON THE TIMING BOARD). THEREFORE, THE PROCEDURE BELOW IS FOR TROUBLESHOOTING AND THEN INTEGRATED CIRCUIT REPLACEMENT.

1) UL1 -

AT J1 CHECK THE PRESENCE OF 4 PULSES PER CYCLE OF OPERATING FREQUENCY. REPLACE UL1 IF NOT AS ABOVE. IF STILL NOT CORRECT REPLACE UL2.

2) UL3 -

AT J2 CHECK THE PULSES VS. THOSE AT J1.

FR (1+2), $\overline{X5}$	J2 IDENTICAL J1	
FR (1+2), X5	J2 ONE HALF J1	
FR (3+4), $\overline{X5}$	J2 IDENTICAL J1	
FR (3+4), X5	J2 ONE FIFTH J1	
FR (5+6), $\overline{X5}$	J2 439 HZ	UNRELATED TO J1
FR (5+6), X5	J2 88 HZ	

IF INCORRECT, REPLACE UL3. IF STILL NOT CORRECT, REPLACE UL2.

3) UL4, UL8 (A,B), UL6A

PUT BOARD #16 ON AN EXTENDER. OBSERVE THE LINE AT COMMON OF CR23, CR22, R23. THE TIME AT 'GROUND' IS THE 'OPERATE' (INTEGRATE) TIME OF THE ANALYZER.

THIS TIME SHOULD CHECK AGAINST THE CHART OF PAGE 5.16-3 AS FOLLOWS:

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3) UL4, UL8 (A,B), UL6A

THE ANALYZER IS SET FOR 2.00 HZ WITH 'X5 OUT'. THE TIMING SHOULD CAUSE OPERATE TIME TO EQUAL 2/F = 1.00 SECOND. (IN 3RD FREQUENCY RANGE, ANALYZE FOR 2 CYCLES TEST FREQUENCY).

THE CHART CAN THUS BE REPRESENTED AS:

FR	'X5 INT'	INTEGRATE TIME
(1+2)	OUT	1/F
(1+2)	IN	2/F
(3)	OUT	2/F
(3)	IN	10/F
(4)	OUT	20/F
(4)	IN	100/F
(5+6)	OUT	.18 SEC.
(5+6)	IN	.90 SEC.

F = FREQUENCY IN HZ.

GREAT CARE MUST BE TAKEN TO SQUARE THE SHORT TIME PULSE AS THE ANALYZER GOES FROM HOLD TO RESET.

IF TIME JUMPS MORE THAN 1/2% OF VALUE FROM RUN TO RUN AT THE SAME FREQUENCY, THERE IS A PROBLEM.

CONTINUE AS IN (1) AND (2). REPLACE UL4, THEN UL8, AND THEN UL6.

UL7A MAY MALFUNCTION AND EFFECT OPERATE TIME. THEREFORE, IT TOO SHOULD BE REPLACED AS A STEP IN TIMING CORRECTION.

IF A FACTOR IS WRONG, CHECK LOGIC LEVELS AT PINS A, D, C, 3, 4, 21, B OF BOARD #16. IF ONE IS INCORRECT, TRACE IT BACK TO MALFUNCTION IN ANOTHER BOARD.

4) UL5A, UL6B

IF INTEGRATE TIME IS CORRECT, AND ANALYZER GOES INTO 'HOLD', BUT DOES NOT GO INTO 'RESET' (PIN 'L' STAYS AT -15 VOLTS), REPLACE UL6, THEN UL5.

5) UL8 - UL5 - UL7

ANALYZER WILL NOT COME OUT OF 'RESET'. REPLACE UL8, THEN UL5, THEN UL7. CHECK LOGIC LEVELS AT 'W', 'S', 'R', 'K'. IF ONE IS WRONG, CHECK BACK TO SOURCE.

[BE CAREFUL THAT SWEEP HAS NOT REACHED END-OF-SWEEP (DS9 'ON'), OR S5 IS 'OFF'].

6) UL7

IF THE SWEEP DOES NOT COME OUT OF 'HOLD' AFTER RESET IS ENDED, REPLACE UL7.

IF THE RESET FLIP-FLOP UL7A DOES NOT RESPOND TO UL6 TRIGGER, REPLACE UL7.

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916HX

6.10.3 - AUTOMATIC GAIN CONTROL - BOARD #5

REFERENCE: SECTION 4.8, FIG. 4.8-1
DRAWING NO. C103116

SINCE BOARD #5 DOES NOT HAVE ADJUSTMENTS, A MALFUNCTIONING PART MUST BE FOUND AND THEN BE REPLACED.

1) NOISE OVERLOAD RESPONSE - UL6, Q1 THRU Q6

CAUSE NOISE OVERLOAD BY OPERATING 916 ANALYZER AT 800 HZ, 10 VOLT OUTPUT CONNECTED TO BOTH INPUTS. DEPRESS PRESET-GAIN.

PUT BOARD #5 ON AN EXTENDER. CHECK PINS AT 7 AND 9 OF UL6. THEY SHOULD SHOW NOISE OVERLOAD PULSES. IF '7' HAS NO PULSES, REPLACE Q4, Q3, THEN UL6, AND THEN Q6. IF '9' HAS NO PULSES REPLACE Q1, Q2, THEN UL6, AND THEN Q5.

2) SIGNAL OVERLOAD OR SIGNAL UNDERLOAD RESPONSE DOES NOT CHANGE RESPECTIVE INPUT AMPLIFIER GAIN

CH#1 - CHANGE UL3, UL4, UL1. IF THIS DOES NOT CORRECT MALFUNCTION, CHECK PINS L, M & K (BOARD #5 ON AN EXTENDER). PIN 'L' HAS 30 MICROSECONDS PULSE (-15 TO GROUND) AT START OF RESET PERIOD (USE MEMORY SCOPE). PIN 'M' AT GROUND FOR UNDERLOAD, PIN 'K' AT GROUND FOR OVERLOAD. IF ONE OF THESE ARE INCORRECT, TRACE BACK TO BOARD #11 FOR RESET PULSE, BOARD #12 FOR OVERLOAD AND UNDERLOAD.

CH#2 - CHANGE UL3, UL2. IF THIS DOES NOT CORRECT MALFUNCTION, CHECK PINS 'L', 'R', 'N' (BOARD #5 ON AN EXTENDER). PIN 'L' HAS 30 MICROSECONDS PULSE (-15 TO GROUND) AT START OF RESET PERIOD (USE MEMORY SCOPE). PIN 'N' AT GROUND FOR UNDERLOAD, PIN 'R' AT GROUND FOR OVERLOAD. IF ONE OF THESE ARE INCORRECT, TRACE BACK TO BOARD #11 FOR RESET PULSE, BOARD #12 FOR OVERLOAD AND UNDERLOAD.

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6.10.3 - AUTOMATIC GAIN CONTROL - BOARD #5

REFERENCE: SECTION 4.8, FIG. 4.8-1
DRAWING NO. C103116

SINCE BOARD #5 DOES NOT HAVE ADJUSTMENTS, A MALFUNCTIONING PART MUST BE FOUND AND THEN BE REPLACED.

1) NOISE OVERLOAD RESPONSE - UL6, Q1 THRU Q6

CAUSE NOISE OVERLOAD BY OPERATING 916 ANALYZER AT 800 HZ, 10 VOLT OUTPUT CONNECTED TO BOTH INPUTS. DEPRESS PRESET-GAIN.

PUT BOARD #5 ON AN EXTENDER. CHECK PINS AT 7 AND 9 OF UL6. THEY SHOULD SHOW NOISE OVERLOAD PULSES. IF '7' HAS NO PULSES, REPLACE Q4, Q3, THEN UL6, AND THEN Q6. IF '9' HAS NO PULSES REPLACE Q1, Q2, THEN UL6, AND THEN Q5.

2) SIGNAL OVERLOAD OR SIGNAL UNDERLOAD RESPONSE DOES NOT CHANGE RESPECTIVE INPUT AMPLIFIER GAIN

CH#1 - CHANGE UL3, UL4, UL1. IF THIS DOES NOT CORRECT MALFUNCTION, CHECK PINS L, M & K (BOARD #5 ON AN EXTENDER). PIN 'L' HAS 30 MICROSECONDS PULSE (-15 TO GROUND) AT START OF RESET PERIOD (USE MEMORY SCOPE). PIN 'M' AT GROUND FOR UNDERLOAD, PIN 'K' AT GROUND FOR OVERLOAD. IF ONE OF THESE ARE INCORRECT, TRACE BACK TO BOARD #11 FOR RESET PULSE, BOARD #12 FOR OVERLOAD AND UNDERLOAD.

CH#2 - CHANGE UL3, UL2. IF THIS DOES NOT CORRECT MALFUNCTION, CHECK PINS 'L', 'R', 'N' (BOARD #5 ON AN EXTENDER). PIN 'L' HAS 30 MICROSECONDS PULSE (-15 TO GROUND) AT START OF RESET PERIOD (USE MEMORY SCOPE). PIN 'N' AT GROUND FOR UNDERLOAD, PIN 'R' AT GROUND FOR OVERLOAD. IF ONE OF THESE ARE INCORRECT, TRACE BACK TO BOARD #11 FOR RESET PULSE, BOARD #12 FOR OVERLOAD AND UNDERLOAD.

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6.11 - HIGH FREQUENCY ACCURACY

1) INTRODUCTION

THERE ARE SEVERAL STEPS THAT WERE TAKEN TO INSURE THAT THE MODEL 916XH IS ACCURATE AT 10 TO 100 KHZ.

THIS INCLUDES:

(A) SPECIAL ADJUSTMENT OF THE D.C./FREQUENCY CONVERTER IN THE 100 KHZ F.S. FREQUENCY RANGE.

(B) PHASE SHIFT OF THE TRIANGULAR WAVEFORM MAKE SIN AND COS REFERENCES 90° TO 100 KHZ.

(C) PHASE CORRECTION OF THE INPUT AMPLIFIERS FOR PHASE RESPONSE TO 100 KHZ AT HIGHER GAINS MATCHING THAT AT LOW GAIN.

(D) PHASE MATCH OF PREAMPLIFIER.

2) D.C./FREQUENCY CONVERTER

SECTION 6.3.3.1 COVERED THE HIGH FREQUENCY ADJUSTMENT OF FREQUENCY VS. DCS1.

3) SPECIAL CONSIDERATIONS

1) IN THE HIGH FREQUENCY RANGE (10 KHZ TO 100 KHZ), THE OUTPUT AMPLIFIER WHICH GENERATES THE TEST SIGNAL, HAS SIGNIFICANT PHASE SHIFT AND ATTENUATION.

THEREFORE THE TEST SIGNAL AND THE 'COS' REFERENCE CANNOT BE COMPARED FOR 90° PHASE DIFFERENCE.

2) IN THE HIGH FREQUENCY RANGE (10 KHZ TO 100 KHZ), THE TEST SIGNAL MAY BE USED AS THE RETURN SIGNAL TO BOTH CHANNELS OF THE ANALYZER, AND EITHER '0°' OR '180°' CHECKED OVER THE AMPLITUDE RANGE OF THE 916.

IF AN 'ATTENUATOR' IS USED TO MAKE THE RETURN SIGNAL TO CH#2 DIFFERENT FROM THAT OF CH#1, GREAT CARE MUST BE TAKEN THAT THE ATTENUATOR'S PHASE SHIFT BE SMALL COMPARED TO THE PHASE SHIFT BEING CHECKED.

AT PRESENT WE RECOMMEND THE DEKAVIDER FROM ELECTRO SCIENTIFIC INDUSTRIES - DV411A - USED OVER '0' TO '60' DB ATTENUATION.

6.11 - HIGH FREQUENCY ACCURACY - CONT'D.

4) PREAMPLIFIERS - LEFT FRONT CABLE

THE FINAL ADJUSTMENT IS OF THE 4 INPUT TRIM CONDENSERS (REFERENCE: DRAWING NO. C102992-2) C3, C7, C11, C17.

OPERATE THE 916XH AT 100 KHZ AND 10 VOLT OUTPUT CONNECTED TO CH#2 AND CH#1 '+' INPUTS ('-' INPUTS AT GROUND). USE 'X5' IN.

USE C11 TO MAKE THE PHASE READOUT IDENTICAL TO THAT AT 5 KHZ (SWITCH FREQUENCY RANGE. LEAVE R1 AT FULL SCALE) (NEAR ZERO PHASE).

MOVE CH#2 INPUT TO '-' AND GROUND '+'. USE C7 TO MAKE PHASE READOUT AGREE WITH 5 KHZ (NEAR 180.0°).

MOVE CH#1 INPUT TO '-', AND GROUND '+'. USE C17 TO MAKE PHASE READOUT AGREE WITH 10 KHZ (NEAR ZERO '°').

IF AT ANY STAGE THE CONDENSER DOES NOT HAVE SUFFICIENT RANGE, MOVE C3 TO A NEW SETTING AND TRY AGAIN.

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7. - FAST CHECKOUT & CALIBRATION

7.1 - PURPOSE

BEFORE A MODEL 916 IS USED, IT IS IMPORTANT TO KNOW THAT IT IS WORKING WELL. THE FAST CHECKOUT PROCEDURE OF SECTION 7.2 GIVES THE USER THIS CONFIDENCE IN A FEW MINUTES OF SELF-CHECKING.

THE CALIBRATION OF THE MODEL 916 CAN BE IMPROVED BY THE STEPS SUGGESTED IN SECTION 7.3. THIS PROCEDURE IS SUGGESTED FIRST, TO AUGMENT THE CHECKOUT OF SECTION 7.2, AND AS A MEANS TO IMPROVE OPERATION AT VERY POOR SIGNAL TO NOISE RATIOS.

THE PROCEDURES REQUIRE A DVM. ALL OF THE TEST POINTS AND ADJUSTMENTS ARE AVAILABLE AT THE FRONT OF THE PC BOARDS WITH THE FRONT PANEL OPEN.

7.2 - FAST CHECKOUT

CONNECT THE OUTPUT TEST SIGNAL AS THE INPUT TO BOTH CHANNELS OF THE ANALYZER.

STEP 1

SET THE FREQUENCY TO 80 HZ. MAKE THE TEST SIGNAL AMPLITUDE 10.0 VOLT PEAK. THE SWEEP IS IN 'RESET'. CONNECT THE TEST SIGNAL TO BOTH '+' INPUT BNC'S (J1A & J3A). GROUND BOTH '-' INPUT BNC'S (J2A & J4A).

THE METERS SHOULD READ:

AMP CH#1	+20.0 DB	±	.1 DB,
AMP CH#2	+20.0 DB	±	.1 DB,
AMP RATIO	00.0 DB	±	.1 DB,
PHASE	00.0 DEGREES		±1.0°
HZ	80.0 HZ		±1%

OPERATE WITH 'X5' IN 'AND' WITH 'X5' OUT. REPEAT RESULTS.

REPEAT AT LOWER FREQUENCY RANGES OF INTEREST.

7.2 - FAST CHECKOUT - CONT'D.

STEP 2

REDUCE TEST SIGNAL 10/1 BY USING '1' VOLT F.S. SWITCH (S7).

REPEAT THE RESULTS OF STEP 1. A.R. AND PHASE SHOULD READ AS BEFORE. AMP CH#1 AND AMP CH#2 SHOULD READ 00.00 DB ±.2 DB.

STEP 3 *(OMIT IN 10 KHZ AND 100 KHZ FREQUENCY RANGES).

CONNECT COS TEST SIGNAL (J11 ON REAR PANEL) AS INPUT CH#2. LEAVE OUTPUT (J5A ON FRONT PANEL) AS INPUT TO CH#1.

PHASE SHOULD READ 90.0° ±1°. REDUCE TEST SIGNAL FROM 10 VOLT, TO 5 VOLT, TO 2.5 VOLT TO 1.0 VOLT.

OBSERVE THE PHASE. IT SHOULD NOT CHANGE BY MORE THAN 1° TO 2.5 VOLT (AND CAN BE ADJUSTED TO MUCH LESS THAN 1° CHANGE TO 1 VOLT).

REPEAT 'X5' 'IN', 'OUT' AND AT SEVERAL FREQUENCIES IN RANGE OF INTEREST.

REPEAT WITH COS TEST SIGNAL TO CH#1 INPUT, AND OUTPUT SIGNAL TO CH#2.

NOTE: STEPS 1, 2 AND 3 CAN BE REDUCED TO A 10 VOLT, 1. VOLT INPUT SWITCH. IF PHASE CHANGE IS WITHIN 1°, IT WILL HOLD FOR OTHER INPUT LEVELS.

IF THE ABOVE TESTS ARE MET WITHIN THE ±1° LIMITS, THE 916XH IS READY TO USE AND IS WITHIN CALIBRATION LIMITS.

NOTE: 100 KHZ FREQUENCY RANGE

IF THE ABOVE TESTS ARE PERFORMED ABOVE 1 KHZ, AN ADDITIONAL PHASE SHIFT AND ATTENUATION IS PRESENT DUE TO OUTPUT AMPLIFIER CHARACTERISTICS.

ABOVE 1 KHZ OMIT STEP 3.

USE STEP 2, AND READ PHASE SHIFT AND AMPLITUDE RATIO ONLY.

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7.3 - CALIBRATION

STEP 1

MULTIPLIER AND INTEGRATOR ZERO ADJUST - BOARDS #7 & #8

GROUND ALL FOUR INPUTS (J1, J2, J3, J4). OPERATE THE MODEL 916 ANALYZER AT 80 HZ. TURN AUTOMATIC GAIN CONTROL 'OFF' WITH SW20 ON REAR PANEL, A1 OR GROUND J102-12.

READ MULTIPLIER OUTPUT WITH D.C.-DVM ON BOARD #7 FROM J1 TO GROUND (J0 ON BOARD #3, #4).

IF ±5 MV OR MORE, USE R12 TO BRING DOWN WITHIN ±2 MV.

REPEAT FOR J4 USING R36 TO ADJUST WITHIN ±2 MV.

REPEAT FOR BOARD #8.

THEN, READ INTEGRATOR OUTPUTS TO GROUND AT J2 AND J3 OF BOARD #7. PUT ANALYZER IN 'X5' 'IN' OPERATION AT 40 HZ. THE INTEGRATOR OUTPUT SHOULD NOT EXCEED ± 20 MV. IF IT DOES, USE R19 TO ADJUST MAXIMUM EXCURSION OF J2 TO UNDER ±5 MV.

REPEAT WITH R52 FOR J3.

REPEAT FOR BOARD #8.

THIS COMPLETES THE MAJOR STEP IN FAST CALIBRATE.

STEP 2

ZERO PHASE, 180° PHASE

IF ZERO PHASE CHECK OF 7.1-STEP1, WAS OFF BY MORE THAN 1°, PROCEED AS FOLLOWS:

OPERATE AT 80 HZ, 10.0 VOLT OUTPUT SINE WAVE TO BOTH INPUTS. CONNECT OUTPUT TO J1A AND J3A (+ INPUTS).

ADJUST R50 OF BOARD #13 UNTIL M2 READS 00.0 DEGREES.

MOVE INPUT TO J4A (GROUND J3A). IF PHASE READS MORE THAN ±1° FROM 180.0°, USE R47 OF BOARD #13 TO MAKE METER 2 READ EXACTLY 180.0°.

STEP 3

PHASE VS. AMPLITUDE

IF THE CHECKOUT OF 7.2-STEP 3 DID NOT CHECK WITHIN SPECIFICATION (PHASE CHANGED MORE THAN 1° AS AMPLITUDE WAS REDUCED TO 10% OF FULL SCALE - AGC OFF), IT CAN BE CORRECTED AS FOLLOWS:

REPEAT THE STEP OF 7.2-STEP3.

READ PHASE SHIFT CH#1 AT FULL SCALE. ADJUST PHASE AT 10% OF FULL SCALE INPUT USING R55 BOARD #13.

REPEAT WITH CH#2 AT FULL SCALE. THEN, AT 10% OF FULL SCALE, USE R55 BOARD #14 TO HOLD PHASE READING CONSTANT.

COS TEST SIGNAL IS INPUT TO OTHER CHANNEL. AUTOMATIC GAIN CONTROL IS OUT. PHASE WILL READ (TYPICALLY) 90.3° AT FULL SCALE. ADJUST AT 10% TO READ 90.3°. DO ADJUSTMENT FOR CHANNEL THAT IS AT 10% LEVEL.

STEP 4

AMPLITUDE LINEARITY

THE AMPLITUDE CH#1 OR CH#2 IS INCORRECT AT 10% OF FULL SCALE.

SET ANALYZER WITH OUTPUT CONNECTED BACK TO BOTH INPUTS. OPERATE AT 80 HZ, 'X5' 'IN'. HOLD AUTOMATIC GAIN CONTROL 'OUT'.

READ AMPLITUDE AT J1 OF BOARDS #13 AND #14 WITH 10.0 VOLT FULL SCALE INPUT, (CHECK 10.0 VOLT LEVEL USING .2% OR BETTER AC-DVM).

REDUCE TEST SIGNAL TO 10.0% OF PREVIOUS INPUT. S7 CAN BE USED FOR THIS PURPOSE.

BAFCO, INC. 717 MEARNS RD., WARMINSTER, PENNA., 18974

TEL: 215-674-1700
TWX: 510-665-6860

916XH

READ AMPLITUDE AT J1 OF BOARDS #13 AND #14. USE R54 ON EACH BOARD TO MAKE IT PRECISELY 10.0% OF FULL SCALE READING (AS .500 VOLT VS. 5.000 VOLT FULL SCALE).

THIS COMPLETES THE FAST CHECKOUT AND ADJUSTMENT.

NOTE THAT 7.3 ONLY NEED BE DONE AS FAR AS 7.2 SHOWED IT NECESSARY.

REF	ITEM	ASSEMBLY	SUB ASSEMBLY	PARTS LIST	SCHEMATIC	ARTMASTER	MACHINING	REF. DRAWINGS	REF. DRAWINGS
	MODEL 916XH F.R.A.	C102927-12		C102927-12				REAR COVER 101493-3	SWITCH BD. 102994
A1	FRONT PANEL - LEFT		C102927-12	C102927-12	C102992-12	103082	103065	CAL. BD. A103410	SWITCH BD. 102995
A1	CABLE BOARD - LEFT		B102993-12	A103412	C102992-12	102925	102926	BKT. BNC A103393	SWITCH BD. 102996
A1A	CABLE BOARD - LEFT				C102992-12	100085	103652	FIG. 3-1 CONN. DWG.	SWITCH BD. 102997
A1	FRONT PANEL SWITCH BD.		B103414-5	A103415	C102992-12	103029	103033	SHLD BD. 103364	SWITCH BD. 102998
A1	FRONT PANEL PREAMP BD.		C103273-5	C103273-5	C102992-12	103031	103032	SHLD BD. 103030	SWITCH BD. 102999
A2	SWEEP MULTI-DECADE		C102708-12	C102708-12	C102708-12	102709	102710	RES. BD. A103529	SWITCH BD. 103000
A3	INPUT AMPLIFIER CH.1		C103110-12	C103110-12	C103110-12	103084	103085		AUTO PEN LIFT B104102
A4	INPUT AMPLIFIER CH. 2		C103110-12	C103110-12	C103110-12	103084	103085		SHLD. BD. 103641
A5	A.G.C. LOGIC - 2 CH.		C103116	C103116	C103116	103117	103118		SHLD. PRE AMP. 103771
A6	PHASE TRIM & WAVE FORM		C103634-12	C103634-12	C103634-12	103428	103429		REAR BKTS. 103405-2
A7 A8	DUAL MULT. (INTEGRATOR)		C102973-12 C102973-12	C102973-12 C102973-12	C102973-12 C102973-12	102971 102971	102974 102974		REAR ARTMSTR 103404
A9	COSINE GEN. SIN/COS w/LOG		C104473	C104473	C104473	104474	104475		REAR BKT. 103406
A10	DC/FREQUENCY		C104470	C104470	C104470	104471	104472		SHLD. BDS. 103399
A11	X5 INTEGRATE		C103306-1	C103306-1	C103306-1	103307	103308		BKT. BLANK 103407
A12	AMP. & AMP RATIO - db		C103395-5	C103395-5	C103395-5	103396	103397		METER BD. 103891
A13	PHASE & AMPLITUDE - 1		C103401-1	C103401-1	C103401-1	103402	103403		METER BD 103893
A14	PHASE & AMPLITUDE - 2		C103401-2	C103401-2	C103401-2	103402	103403		COVER BD. 104156
A15	7KC BD.		C103046-12	C103046-12	C103046-12	103047	103048		FIG. 4.4-1 BLOCK DIA.
A16	TIMING BD.		C103314-12	C103314-12	C103314-12	103315	103316		FIG. 1-1 FREQ. KHz
A17									FIG. 4.5-2B CORR. CURVE
A18	MULTIPLE REGULATOR		C103376-5	C103376-5	C103376-5	103377	103378		FIG. 4.5-2C CORR CURVE
A19	CABLE BOARD - RIGHT		B103548A	A103549A	C102992-12	103550	103551		FIG. 4-1 BLOCK DIA.
A19	FRONT PANEL SW. BD.				C102992-12	103041	103054	COVER BD. 103356	FIG. 4.4-3 BLOCK DIA
A19	FRONT PANEL - RIGHT		C102927-12	C102927-12	C102992-12	103082	103672		FIG. 4.5-1 BLOCK DIA
	INTERCONNECTION				C103394-12			FIG. 4.5-2A CURVE F.R.	FIG. 4.6-1 BLOCK DIA.
A20	±15V POWER SUPPLY		C103635	C103635	C103636	103621	103622	FIG. 4.8-1 BLOCK DIA	FIG. 4.7-1 BLOCK DIA
	EXTENDER BOARD		100330	100331		101790	101794	FIG. 4.7-1 CURVE	FIG. 4.7-2 BLOCK DIA

REVISIONS

NO	DESCRIPTION	BY	DATE
A	RELEASE		
B	REV. A15. WAS C103046-5		2-81

UNLESS OTHERWISE SPECIFIED
FRACTIONS ± .015
TWO PL. DEC. ± .010
THREE PL. DEC. ± .005
ANGLES ±1/2 DEG.
SUR. FIN. 125 MICROINCH

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BAFCO, INC.

BAFCO, INC

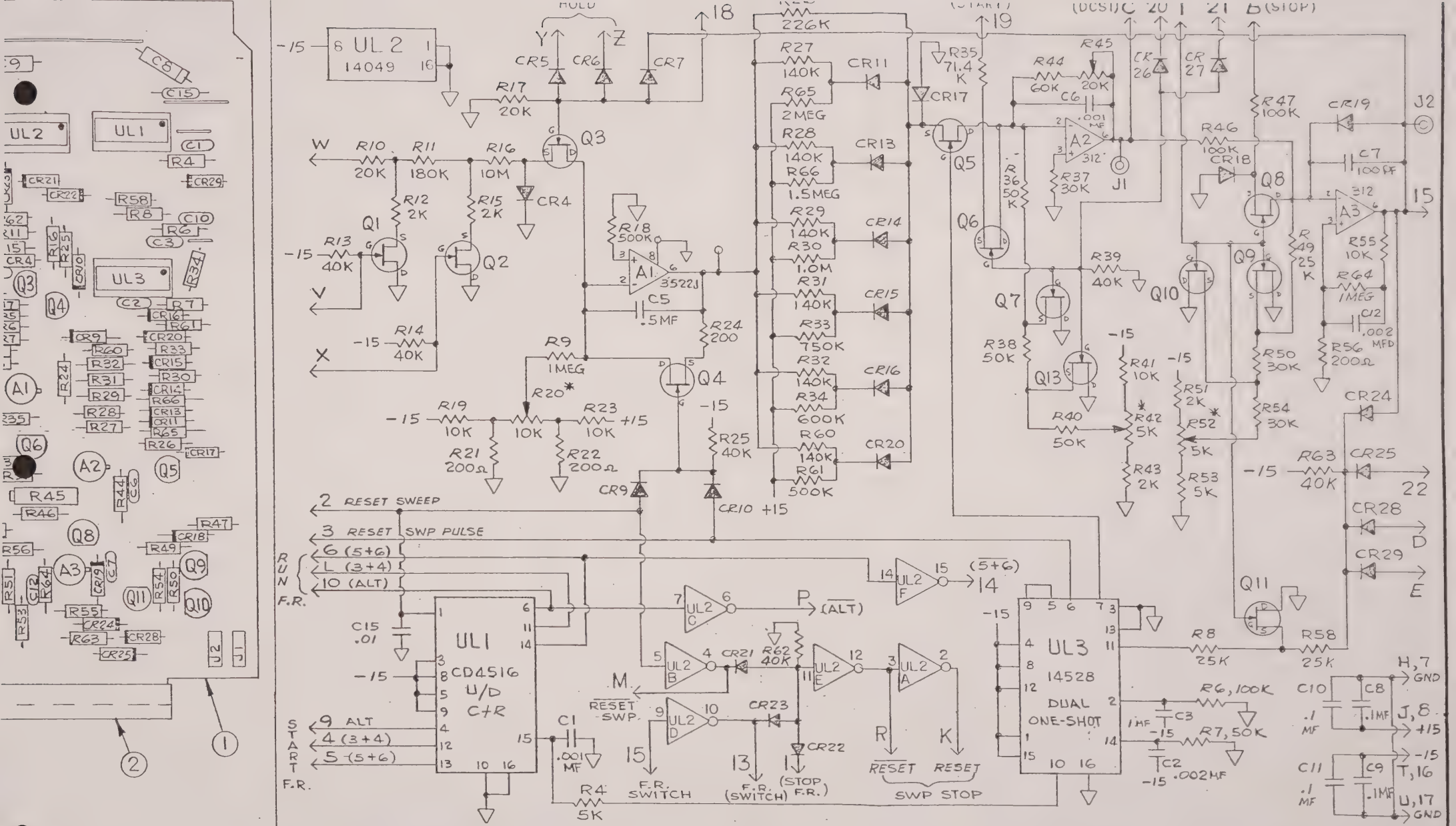
DRAWING LIST
FREQUENCY RESPONSE ANALYZER
MODEL 916XH

BY BRASSI
DATE 31 MAR '81
APPD
DATE

B

SCALE

103400-12



ICATES FRONT OF P.C.
ARD MTG.

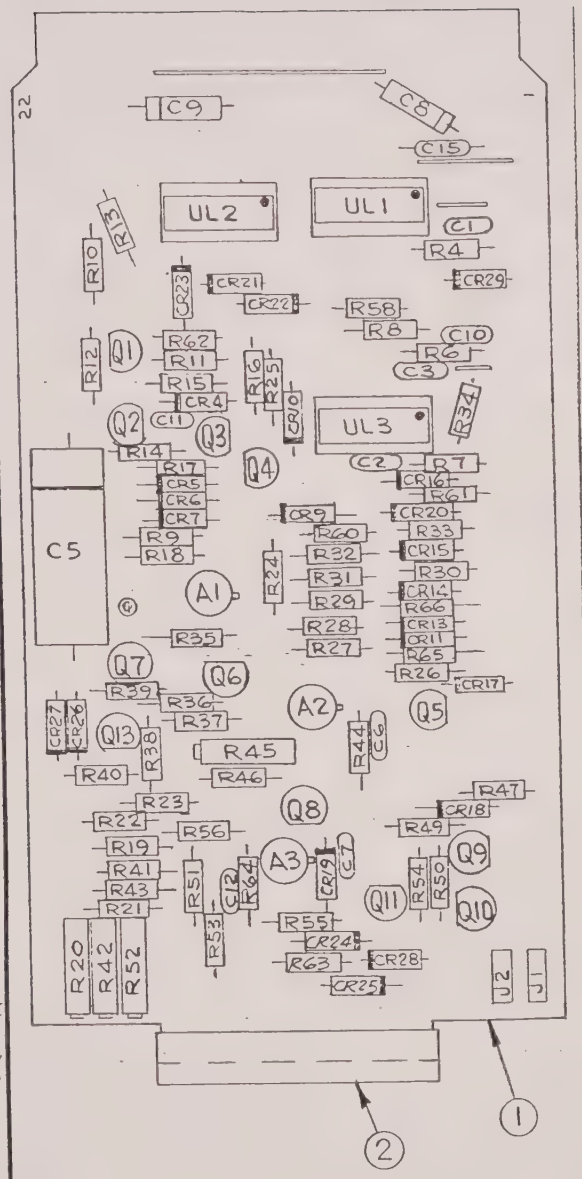
THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	BAFCO, INC	BY GRASSI DATE 12-20-73 APPD DATE	ASSEMBLY #2 SCHEMATIC - SWEEP - MULTI-DECADE MODEL 916XH REF

C | SCALE FULL | 102708-12

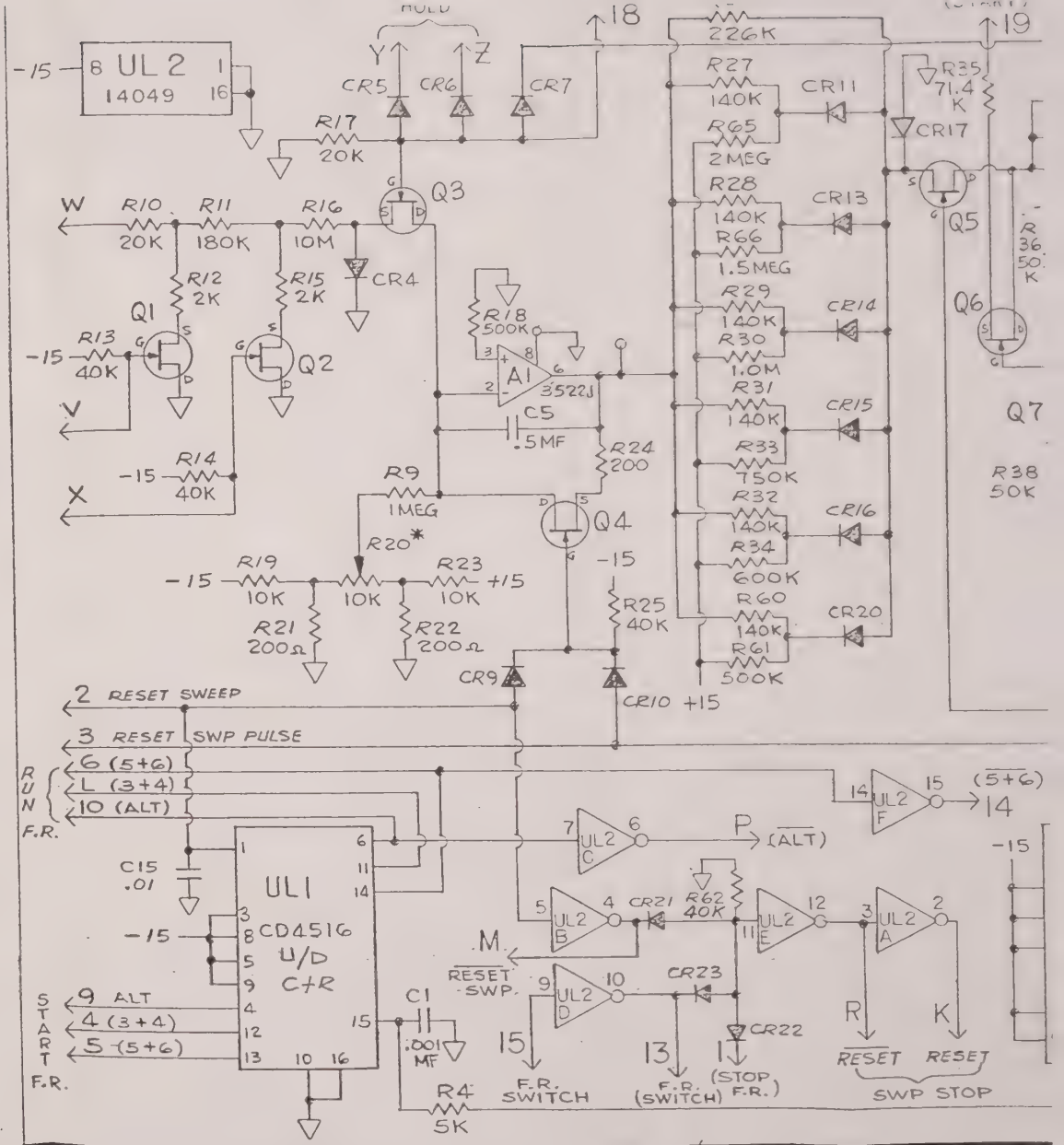
Q	PT NO	DESC	VEND
1	102709	P.C. BOARD	
1	100073	HANDLE	
3	516-AG-11D	I.C. SOCKET	AUGAT
4	M-270	EYELETS	MARK
1	CD4516	I.C. 16 PIN	RCA
1	MC14049	" "	MOT.
1	MC14528	I.C. 16 PIN	MOT.
1		1 MFD	ERIE
1		.5 MFD 100V 10%	S&E I
1		.1 MFD 100V 10%	S&E I
1		.1 MFD	ERIE
1		.1 MFD	"
1	3522J	AMPLIFIER	BURR/BRN
2	LM312	"	NAT'L.
1	LM312	"	"

NOTES:
UNLESS OTHERWISE SPECIFIED;
1- ALL CAPACITORS - ERIE
2- ALL DIODES - FDG6G6 - FAIRCHILD.
3- ALL TRANSISTORS - FET - U1899E SILICONIX
4- ALL RESISTORS - RN60D, 1/4W, 1% CORNING.
5- ALL AMPLIFIERS - NAT'L.

2	RELEASE
NO	REVISIONS



NOTE:
1- * INDICATES FRONT OF P.C. BOARD MTG.



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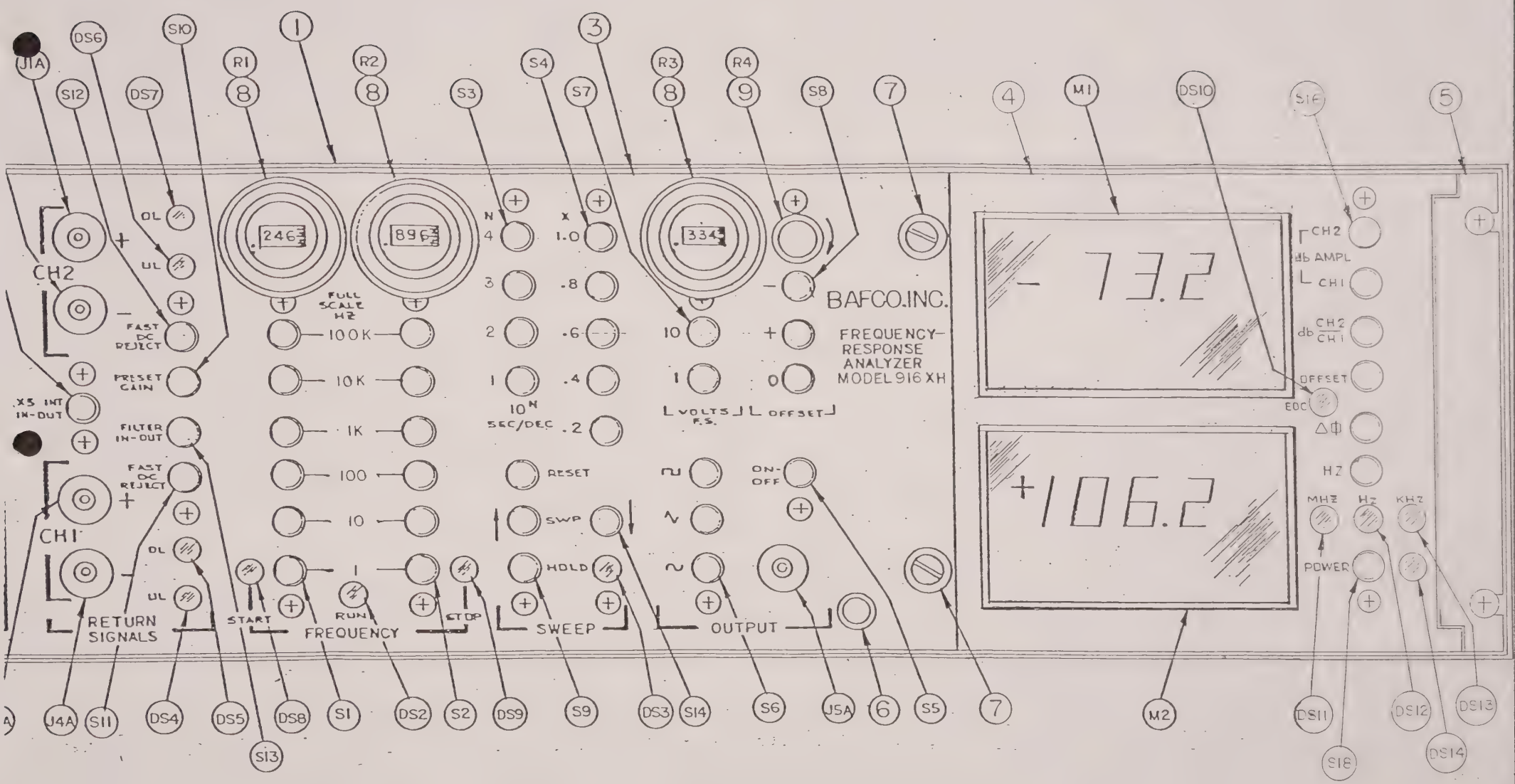
BAFCO, INC.

BAFCO, INC

BY GRASSI
DATE 12-20-73
APPD
DATE

SCHEMATI
MULTI
MODEL 916X



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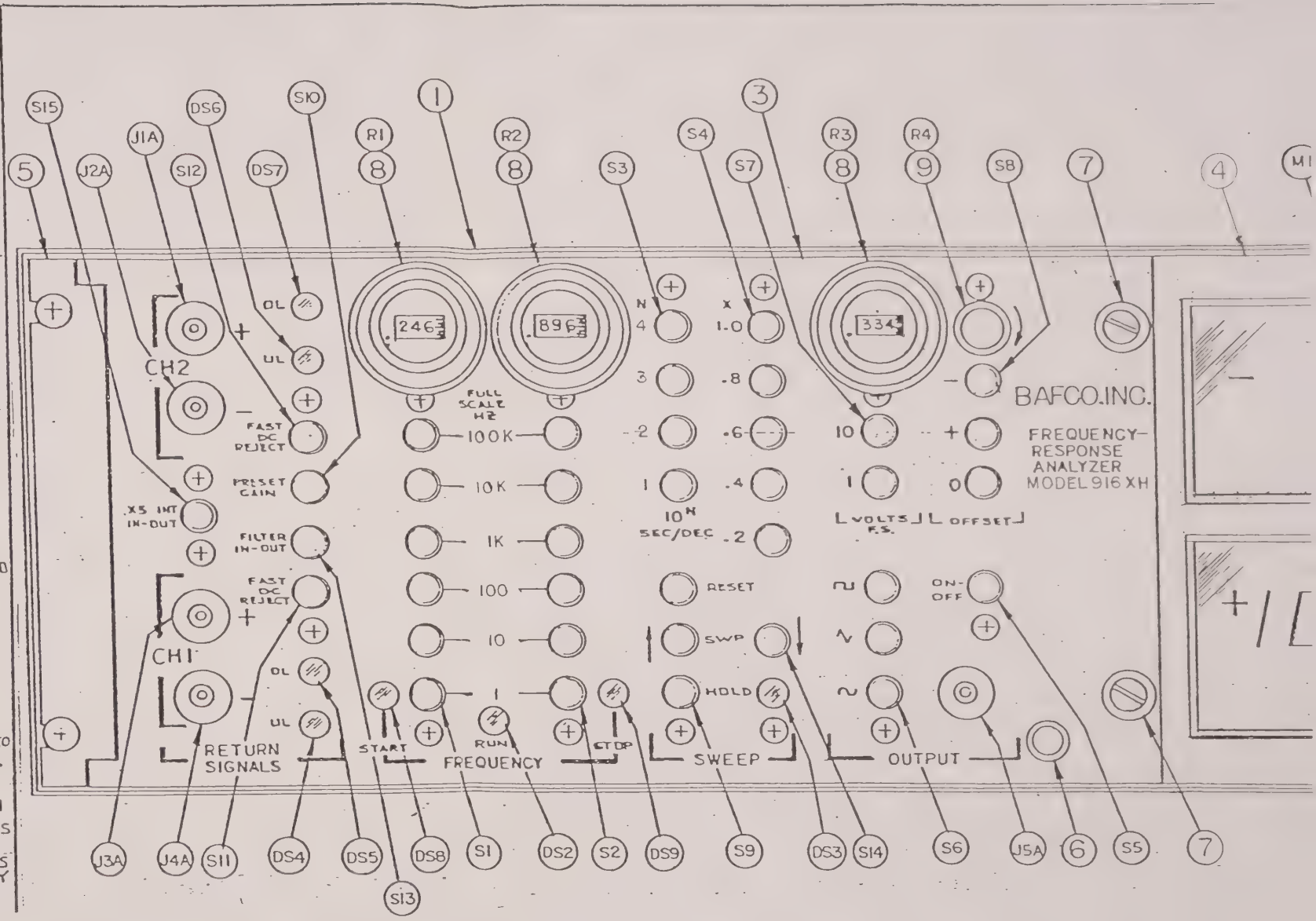
T	G	PT NO	DESC	VEND
1	1	C101492	CASE WELDM'T	BAFCO
2	1	B101493-3	REAR COVER	NOT SHOWN
3	1	B103065	FRONT PNL L.H.	BAFCO
4	1	SEE NOTE 1	FRONT PNL R.H.	"
5	1	A100278	PANEL HINGE	"
6	1	27-10-301-10	LOCK - L.H.	SOUTHCO
7	2	47-10-502-10	LOCK - CAPTIVE	"
8	3	MODEL 3610	KNOB POT	BOURNS
9	1	SDC152	KNOB	
J1A	1	31-010	JACK-BNC	AMPHENOL
J2A	1			
J3A	1			
J4A	1			
J5A	1	31-010	JACK-BNC	AMPHENOL
S1	1	02009-006	SWITCH-6XF12.5	I.E.E.
S2	1			
S3	1	02009-0081	8XF12.5	
S4	1	02009-008	8XF12.5	
S5	1	02009-0061	6XF12.5	
S6	1	02009-006	6XF12.5	
S7	1			
S8	1	02009-0061	6XF12.5	
S9	1	02009-0081	8XF12.5	
S10	1			
S11	1	02009-0041	4XF12.5	
S12	1			
S13	1			
S14	1	02009-008	8XF12.5	
S15	1	02009-001	1XF0003-06	
S16	1			
S17	1	02009-0082	8XF12.5	
S18	1		SWITCH	I.E.E.
DS2	1	MV5153	L.E.D.	MONSANTO
DS3	1			
DS4	1			
DS5	1			
DS6	1			
DS7	1			
DS8	1			
DS9	1			
DS10	1			
DS11	1			
DS12	1			
DS13	1	MV5153	L.E.D.	MONSANTO
DS14	1	2120A1	LAMP	IND.DEV.
M1	1		METER	SEE
M2	1		METER	NOTE 1
R1	1	3610S-1-202	2K POT.	BOURNS
R2	1	3610S-1-202	2K POT.	"
R3	1	3610S-1-502	5K POT	BOURNS
R4	1	1202LB-1	5K POT.	VISHAY



NO	REVISIONS
A	RELEASE

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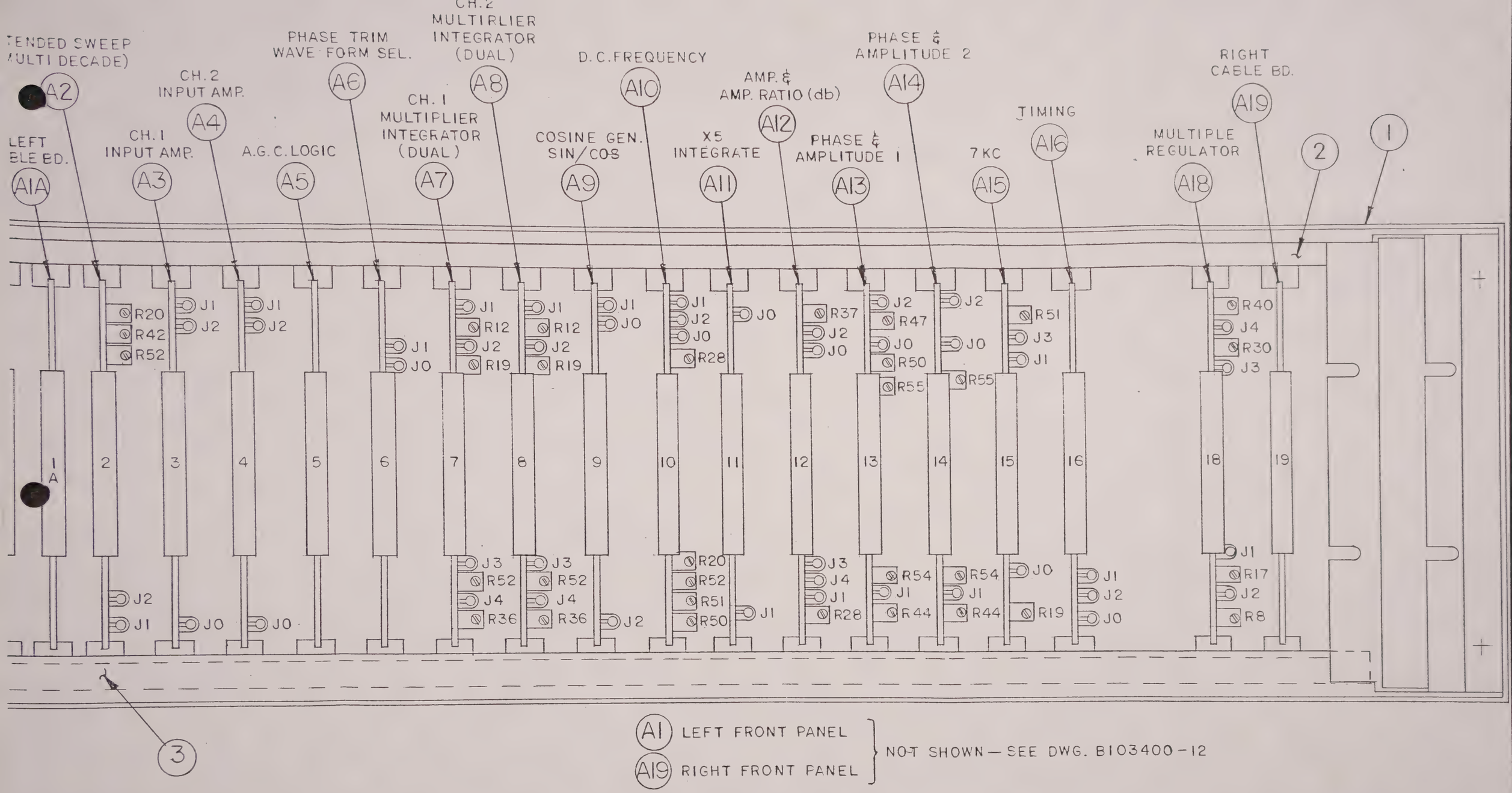
BAFCO, INC.

BAFCO, INC

BY Bressi
DATE 31 MAR '81
APPD
DATE

FREQUENCY R
LEFT/RI
MODEL 916



VIEW WITH FRONT DOORS OPEN

N SCREWS AT EACH END OF BOARD
N BRACKET, ITEM 3, AND MOVE
TO REMOVE P.C. BOARDS.

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BAFCO, INC.

BAFCO, INC

BY JEHASSI
DATE 30 MAR '81
APPD
DATE

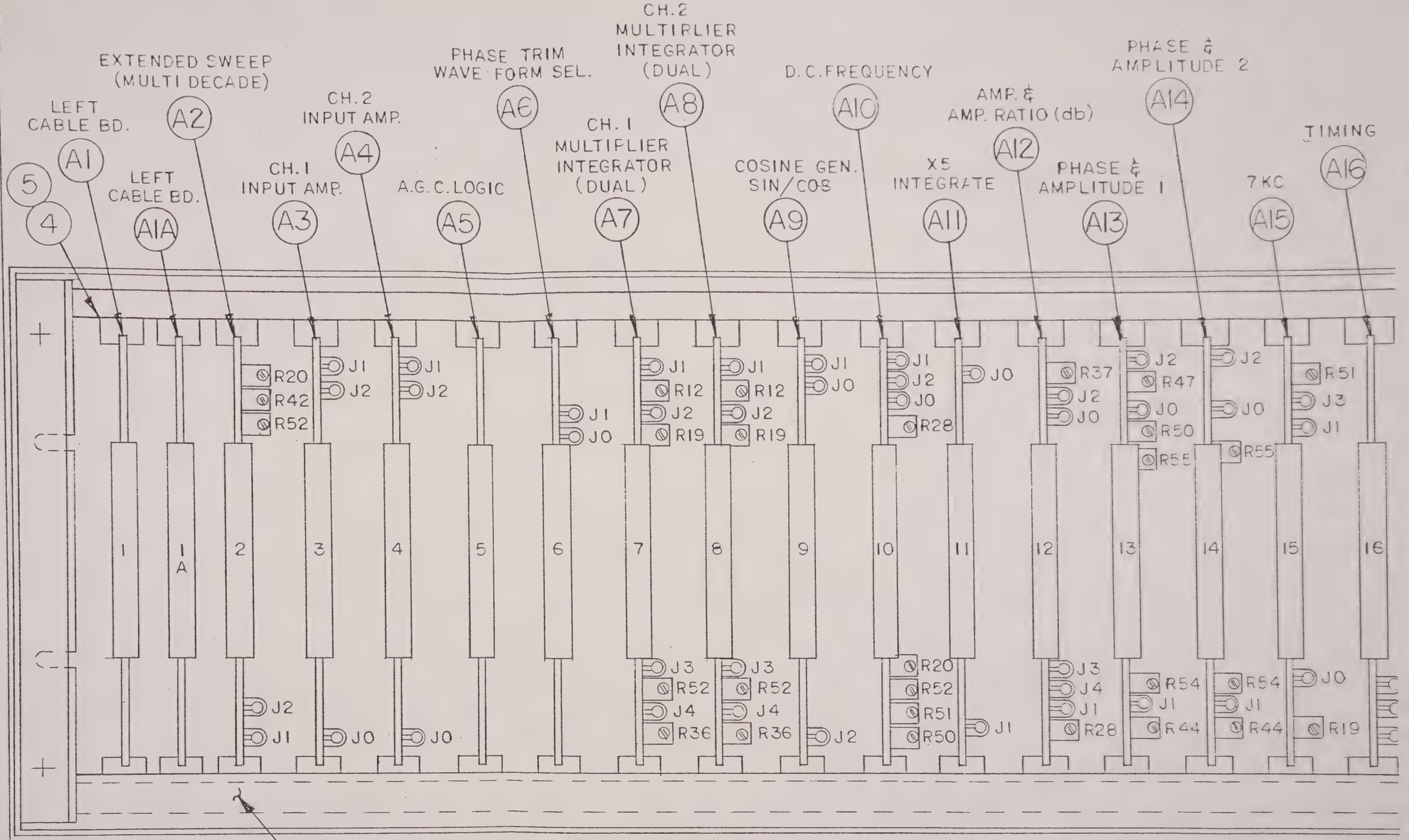
ASSEMBLY
FREQUENCY RESPONSE ANALYZER
MODEL 916XH REF

C

SCALE FULL

102927-12
SH 2 OF 3

IT	Q	PT NO	DESC	VEND
1	1	C101492	CASE WELDM'T	BAFCO
2	1	C100121-B	BD. GUIDE RACK	"
3	1	A101501	BD. R'TN'R BKT.	"
4	1	63-9016-12	BD. GUIDE	ELCO
5	6	9021680043	BD. GUIDE FSTR.	ELCO
6	2	A101499	RACK MTG. BKT.	NOT SHOWN
7	2	1627	HANDLE	"
8	1	1725-S	POWER CORD	BELDEN
A1	1	B102993	LEFT CABLE BD.	BAFCO
A1A	1	100085	LEFT CABLE BD.	
A2	1	102708-12	EXT. SWEEP	
A3	1	103110-12	INPUT AMPL.	
A4	1	103110-12	INPUT AMPL.	
A5	1	103116	AGC	
A6	1	103634-12	WAVE FORM SEL	
A7	1	102973-12	MULT. INT. DUAL	
A8	1	102973-12	MULT. INT. DUAL	
A9	1	104473	COSINE GEN.	
A10	1	104470	DC/FREQ.	
A11	1	103306-1	X5 INT.	
A12	1	103395	AMP. RATIO db	
A13	1	103401-1	PHASE & AMP. 1	
A14	1	103401-2	PHASE & AMP. 2	
A15	1	103046-5	7 KC	
A16	1	103314-12	TIMING BD.	
A18	1	103376-5	MULT. REG.	
A19	1	B103073-A	RT. CABLE BD.	
A20	1	103G35	PS. ±15V.	BAFCO



A1 LEFT FRONT PANEL
A19 RIGHT FRONT PANEL
} NOT SHOWN — SEE DWG.

NOTE:
LOOSEN SCREWS AT EACH END OF BOARD RETAINING BRACKET, ITEM 3, AND MOVE DOWN TO REMOVE P.C. BOARDS.

VIEW WITH FRONT DOORS OPEN

NO	REVISIONS
A	RELEASE

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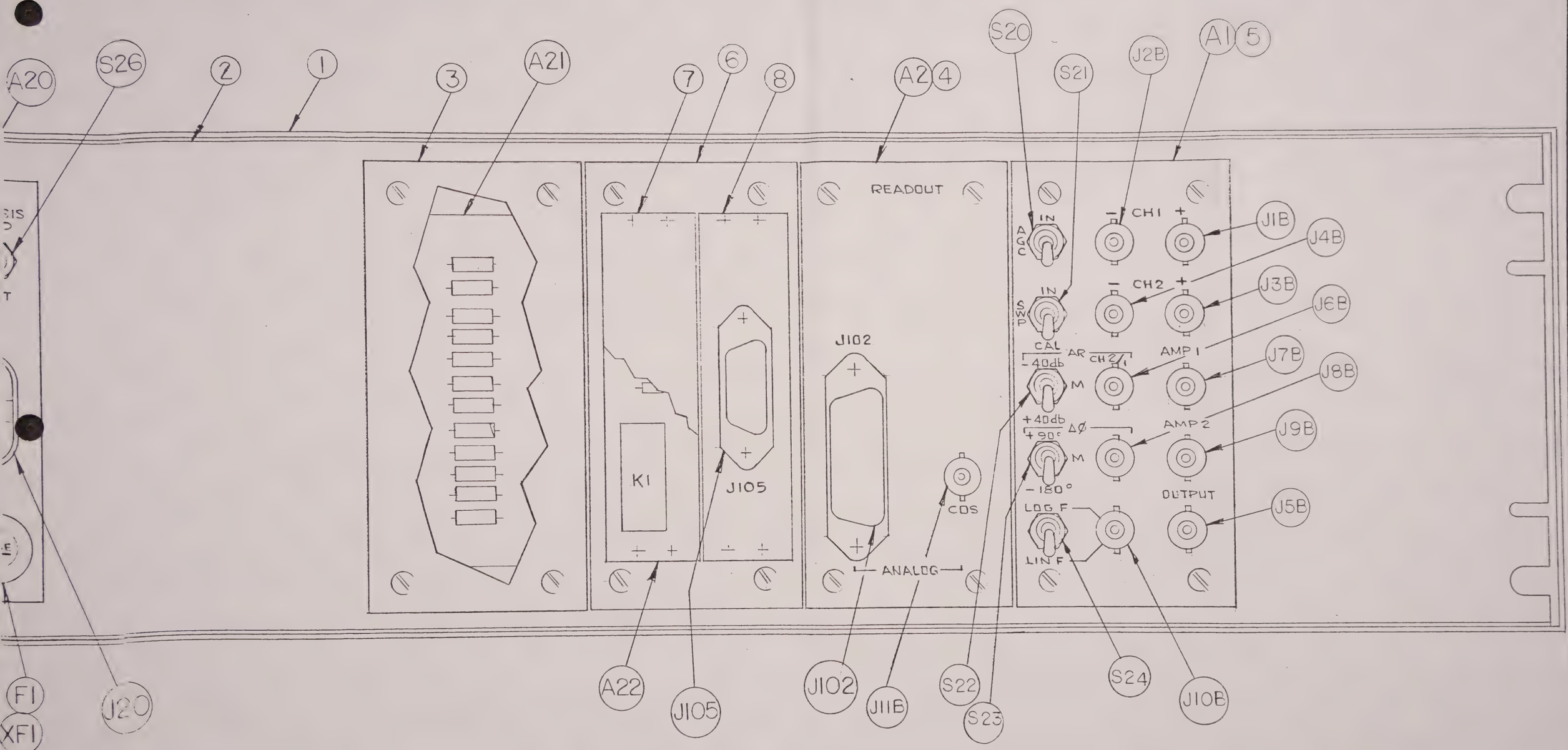
BAFCO, INC.

BAFCO, INC

BY JKASS
DATE 30 MAR '81
APPD
DATE

FREQUENCY

MODEL 91



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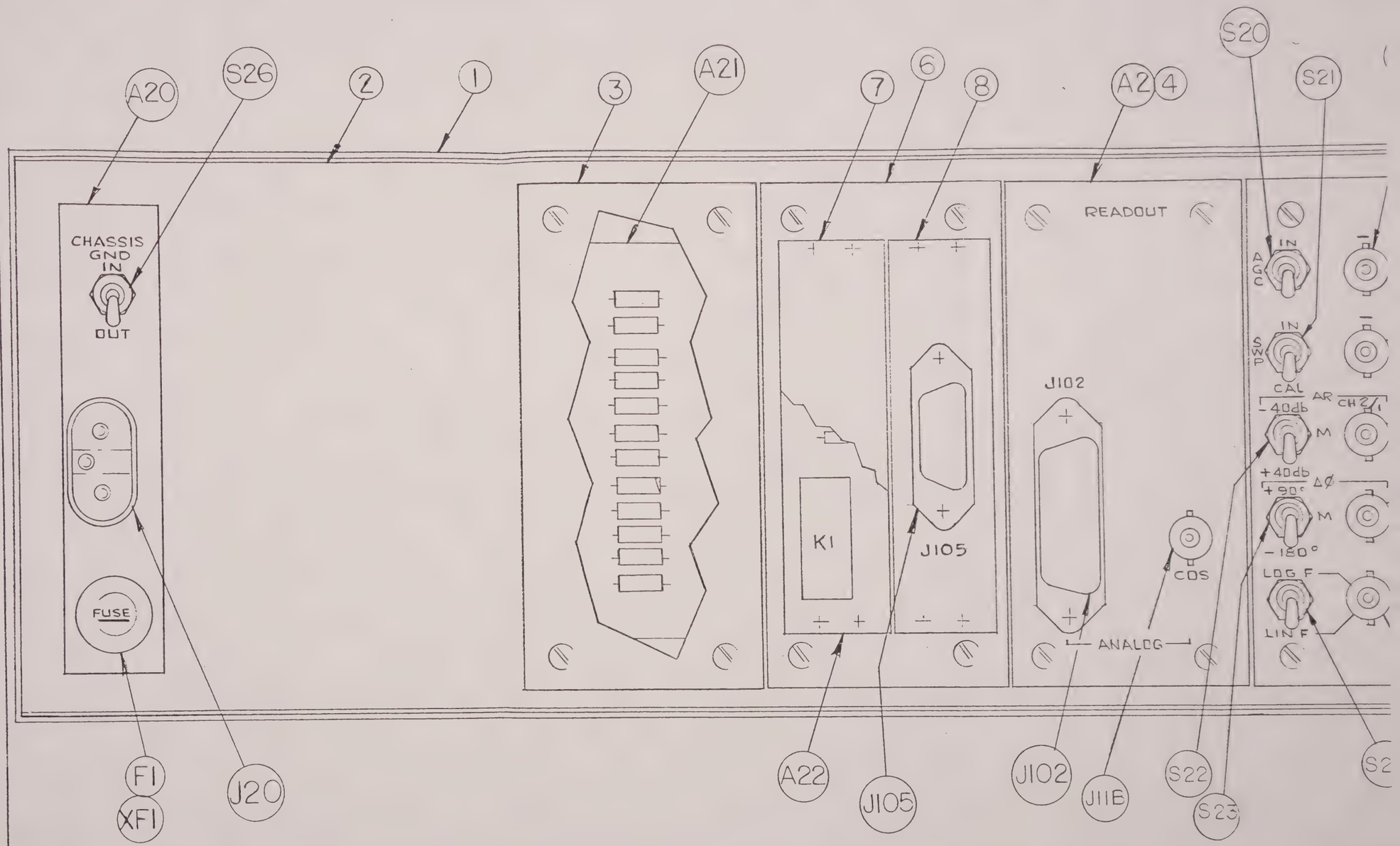
IT	Q	PT NO	DESC	VEND
1	1	C101492	CASE	BAFCO
2	1	B101493-3	REAR COVER	"
3	1	A103407	BKT. BLANK	"
4	1	A103405	BKT. CONN.	"
5	1	A103393	BKT. BNC.	"
6	1	A100537	BKT.	"
7	1	A100784	COVER	"
A21	1	A103531	RES. BD. ASS'Y.	"
A20	1	B103408	P.S. ASS'Y.	BAFCO
S21	1	7208MDE	SWITCH-DPDT	C&K
S22	1	7215MDE	DP 3POS	"
S23	1	7215MDE	DP 3POS	"
S24	1	7101MDE	SPDT	"
S20	1	7108MDE	SWITCH-SPDT	C&K
J6B	1	#31-010	JACK-BNC	AMPHENOL
J7B	1			
J8B	1			
J9B	1			
J10B	1			
J11B	1			
J1B	1			
J2B	1			
J3B	1			
J4B	1			
J5B	1	#31-010	JACK-BNC	AMPHENOL
J102	1	#57-40240	CONN-24PIN	"
8	1	A100782	BKT. CONN	BAFCO
J105	1	#57-40140	CONN.-14 PIN	AMPHENOL
A22	1	B104102	PEN LIFT ASSY.	BAFCO



NO	REVISIONS
A	RELEASE

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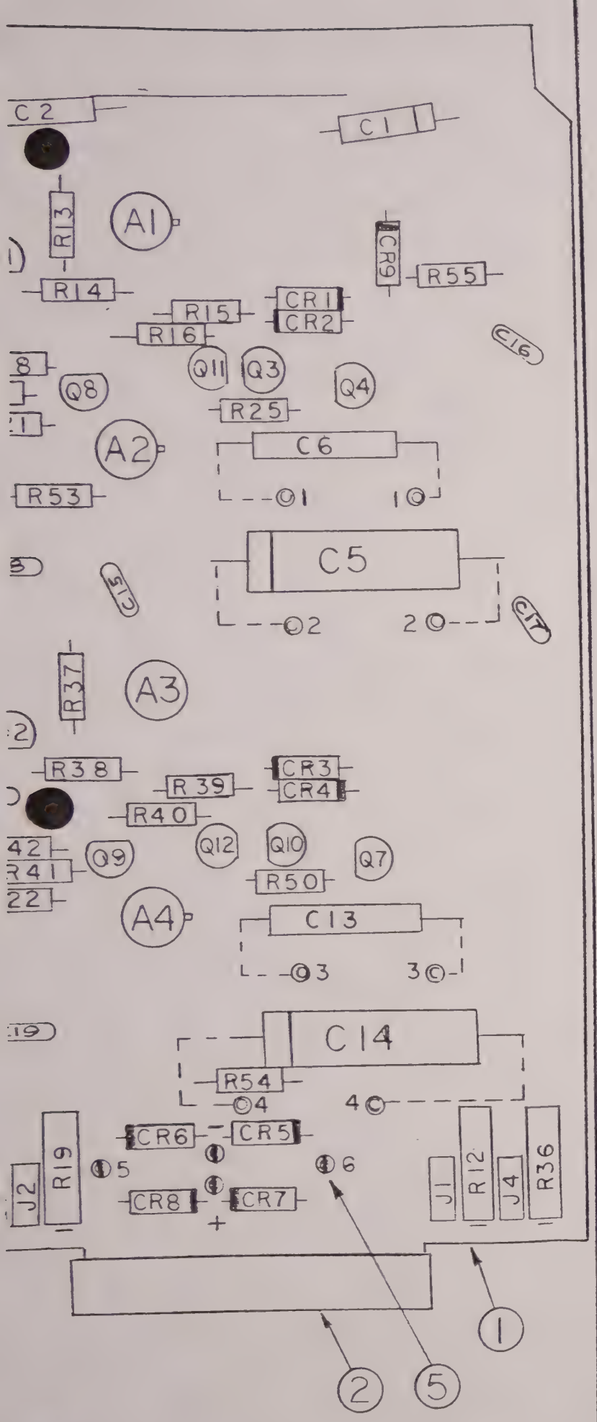
BAFCO, INC.

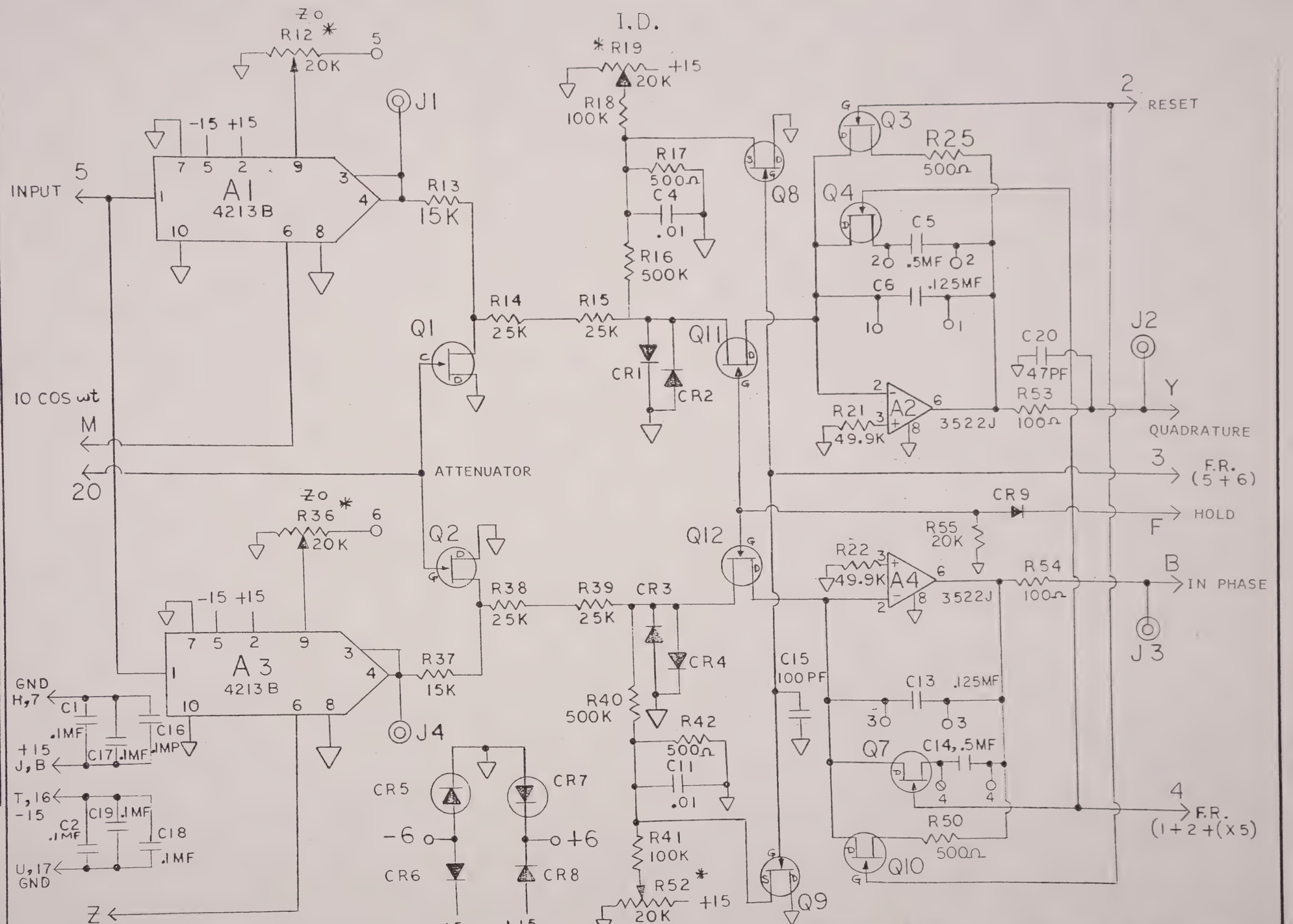
BAFCO, INC

BY ABRASSI
DATE 31 MAR '81
APPD
DATE

FREQUENCY

MODEL 91





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BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

ASSEMBLY (7 & 8)
SCHEMATIC PC BOARD
DUAL MULTIPLIER (INTEGRATOR)
MODEL 916XH **REF**

C

SCALE

102973-12

IT	Q	PT NO	DESC	VEND
1	1	104068	P.C. BOARD	BAFCO
2	1	100073	HANDLE	BAFCO
3	AR	160-1512-02	TURRET LUG	CAMBION
4	4	2926-02	TERMINAL	CAMBION
A1	1	AD632	MULTIPLIER	ANALOG
A3	1			
A2	1	3522J	AMPLIFIER	BURR/BRN
A4	1			
C1	1		.1MFD ±20% 100V	S&EI
C2	1			
C5	1		5 MFD, 50V	S&EI
C14	1			
C6	1		1.25 MFD, 22W	S&EI
C13	1			
CR5	1	IN825	DIODE, ZENER	MOTOROLA
CR6	1	IN5314	DIODE, ZENER	MOTOROLA
CR7	1	IN825	DIODE, ZENER	MOTOROLA
CR8	1	IN5314	DIODE, ZENER	MOTOROLA

NOTES:

1 - UNLESS OTHERWISE SPECIFIED:

ALL RESISTORS 1/4 W, 1%, RN60D, CORNING

ALL CAPS - ERIE

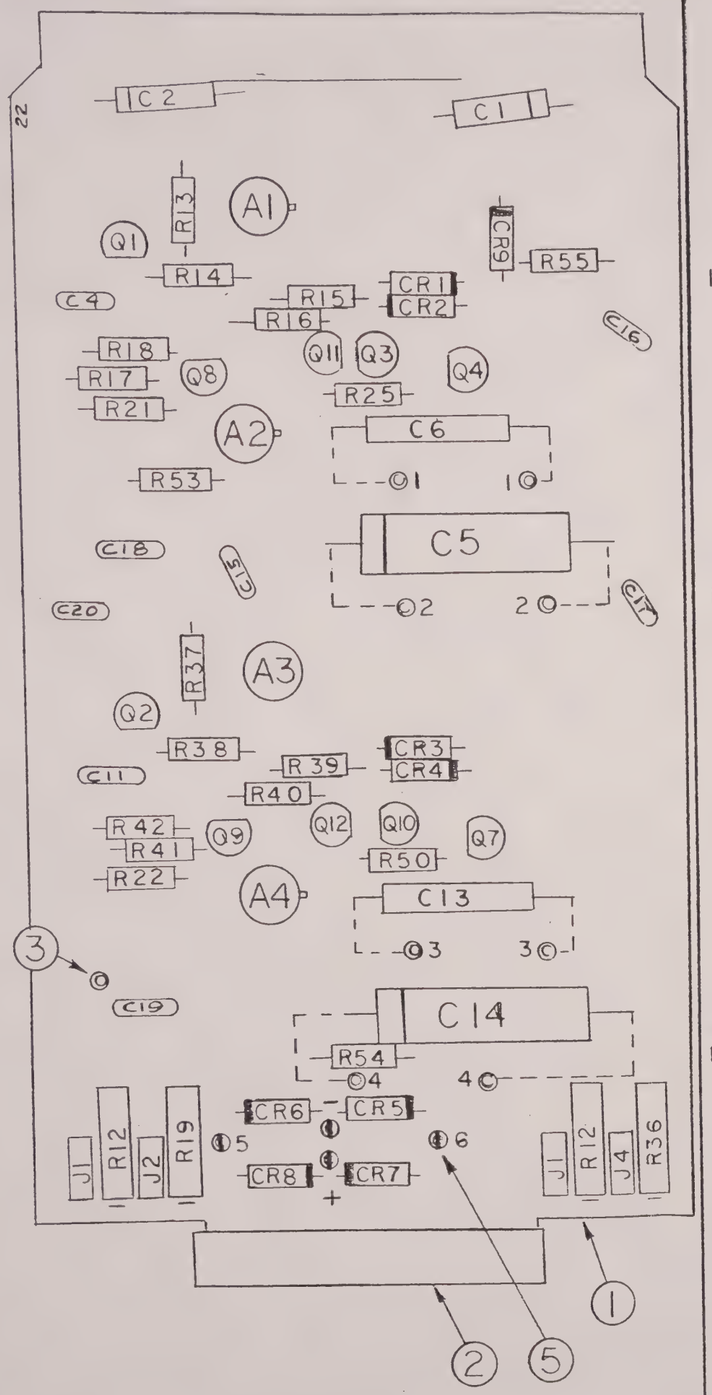
ALL DIODES - FD6666 - FAIRCHILD

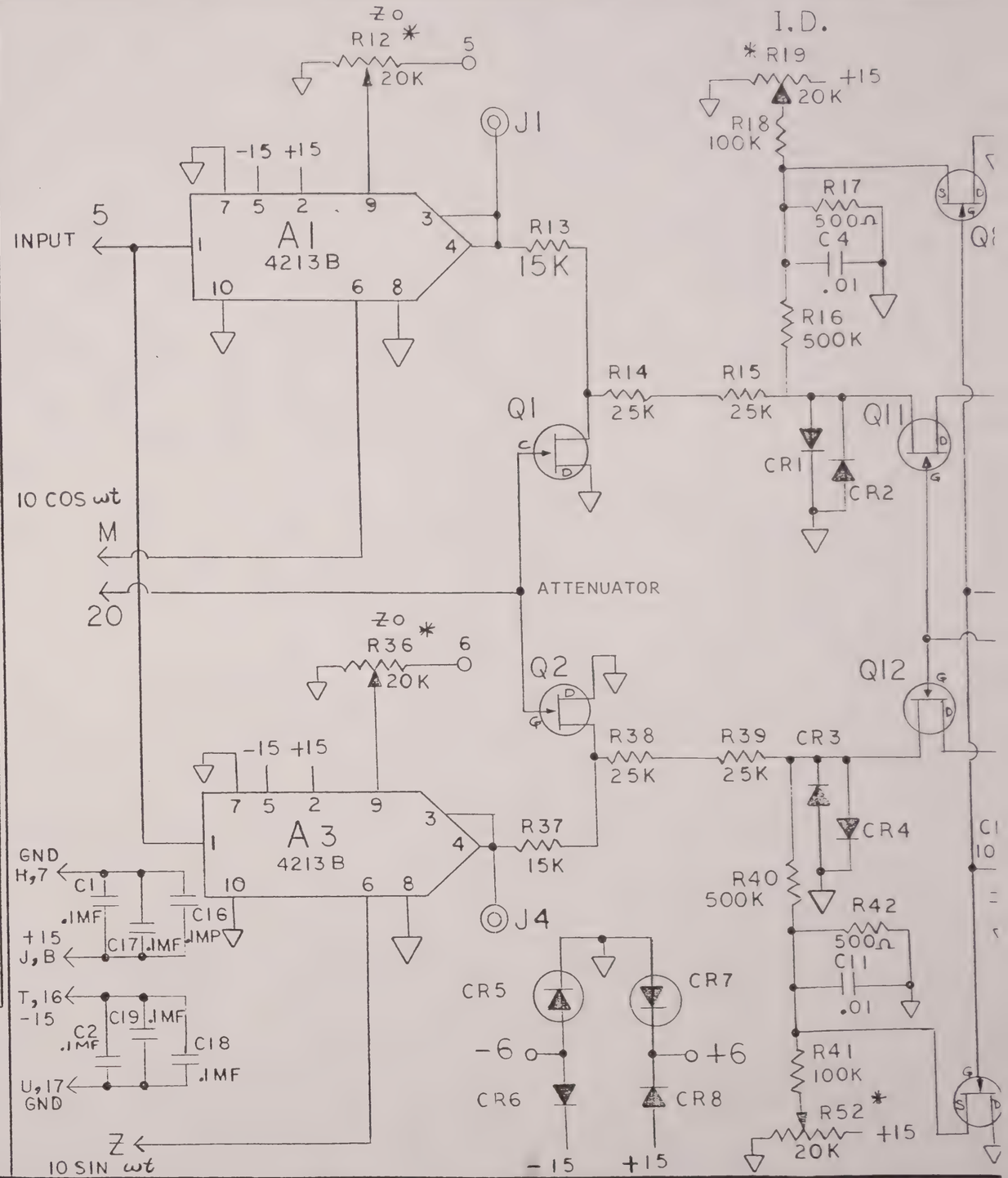
ALL TRANSISTORS - U1899E

ALL VARIABLE POTS - 43P - SPECTROL

ALL JACKS - #430 - H.H. SMITH

NO	REVISIONS
B	REDRAWN 4/82 A.
A	RELEASE
NO	REVSIONS





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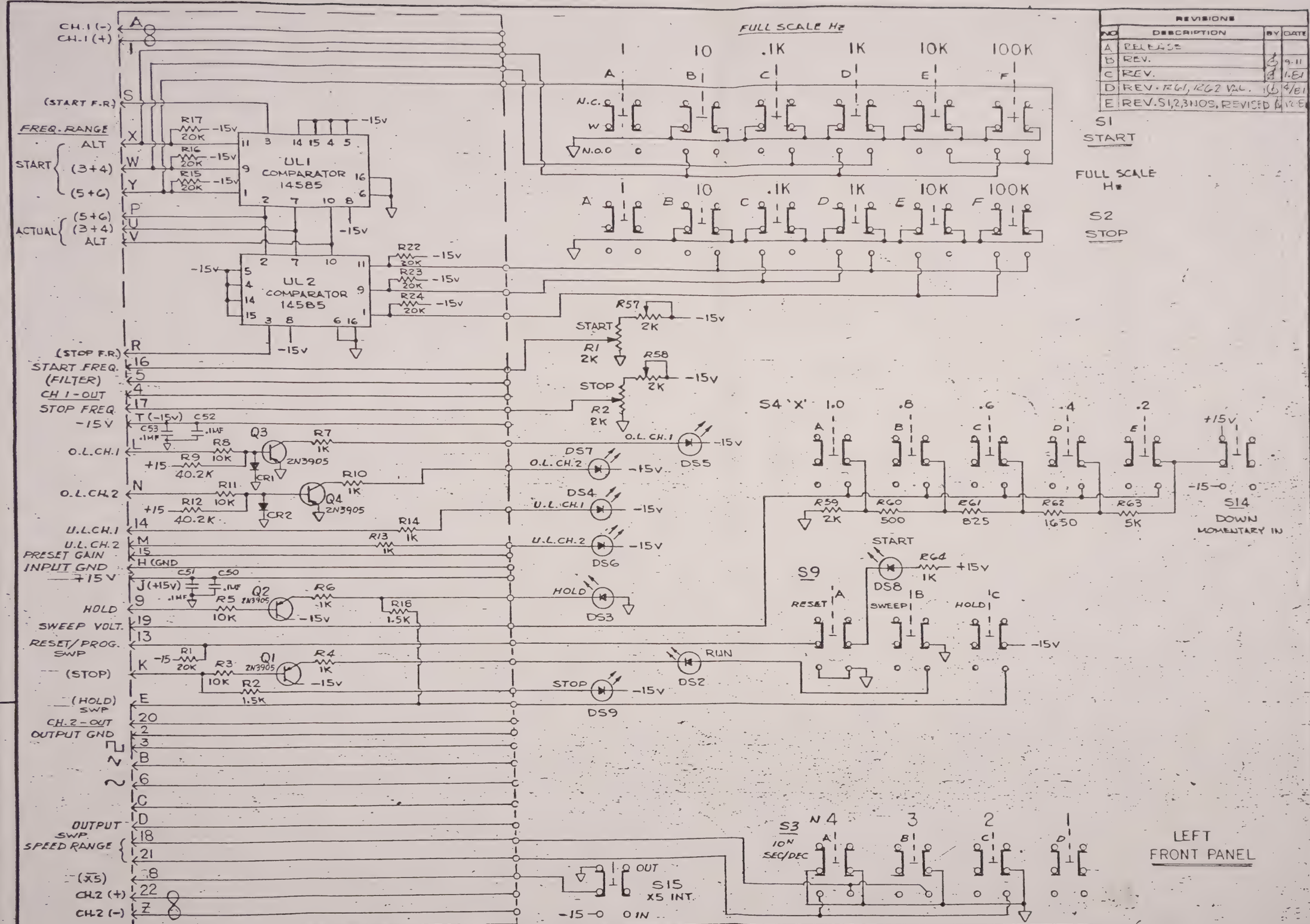
BAFCO, INC.

BAFCO, INC

BY	
DATE	
APPD	
DATE	

A
SCHE
DUAL MUL
MODEL 916X



REVISIONS			
NO	DESCRIPTION	BY	DATE
A	RELEASE		
B	REV.		9-11
C	REV.		1-81
D	REV. R61, R62 VAL.		4/81
E	REV. S1,2,3 NOS. REVISED		12-81

LEFT CABLE BOARD

UNLESS OTHERWISE SPECIFIED
FRACTIONS ± .015
TWO PL. DEC. ± .010
THREE PL. DEC. ± .005
ANGLES ± 1/2 DEG.
SUR. FIN. 125 MICROINCH

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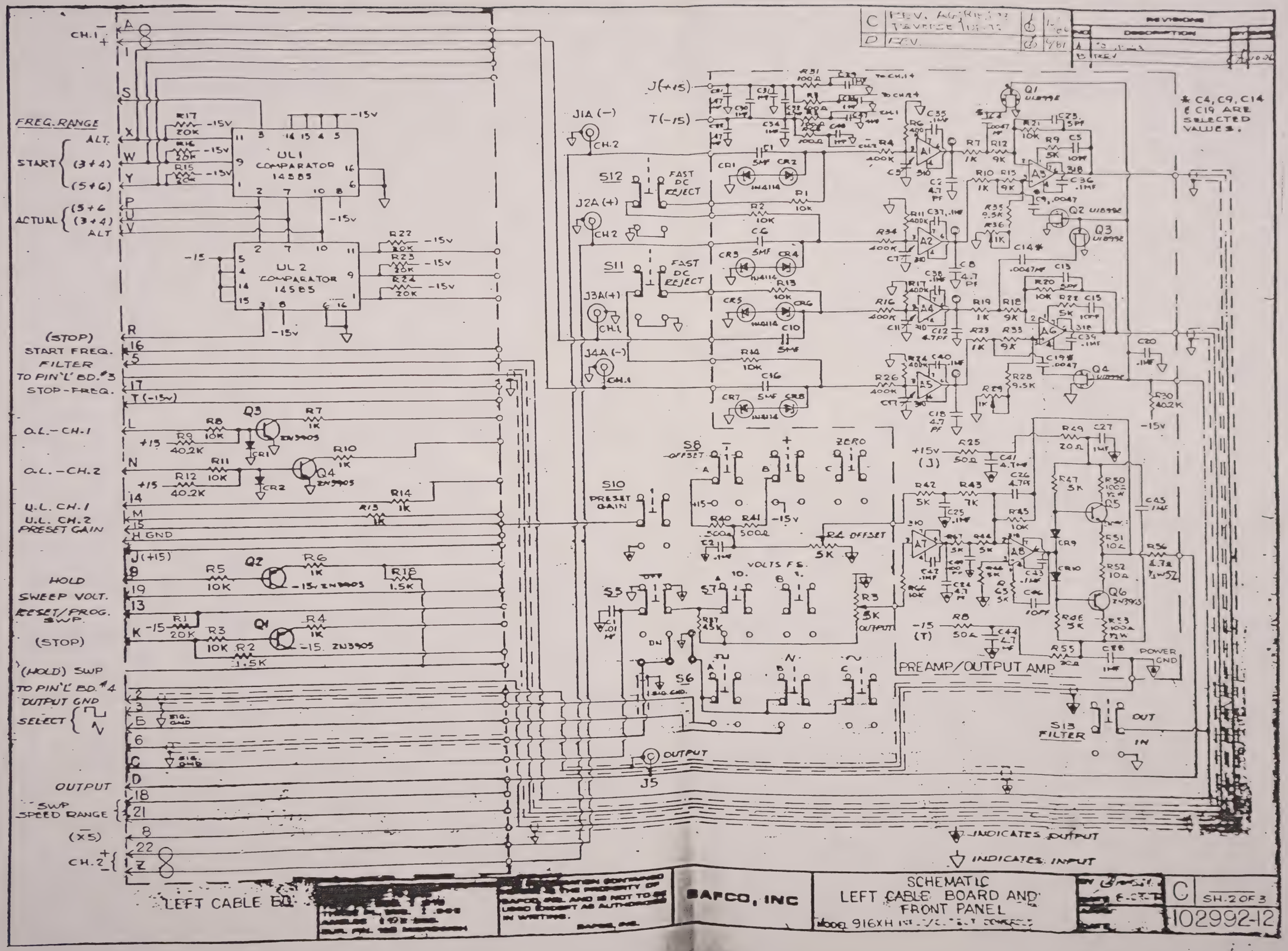
BAFCO, INC

SCHEMATIC
LEFT CABLE BOARD AND FRONT PANEL
MODEL 916XH FREQUENCY & SWEEP CONTROLS

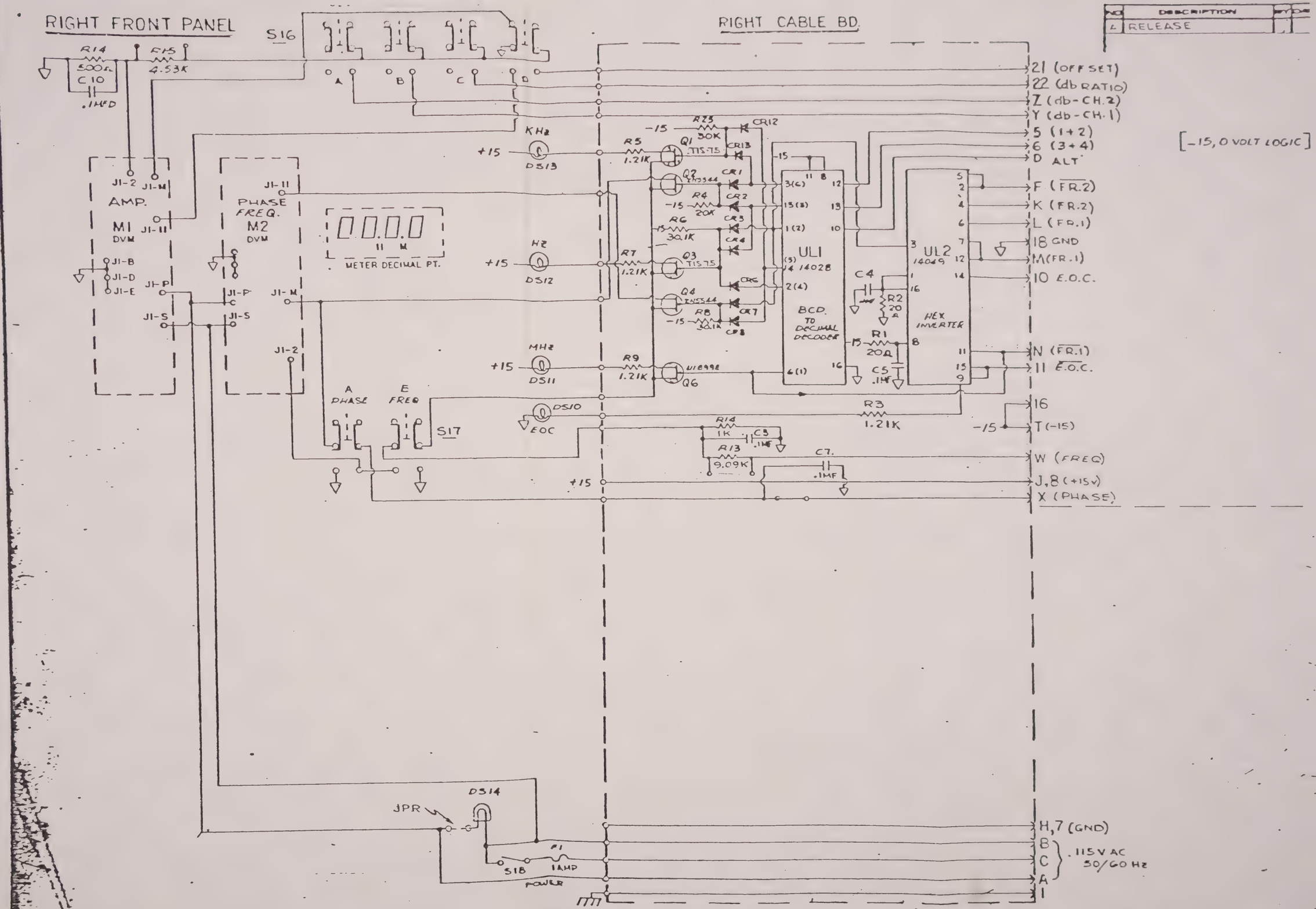
BY Bossi
DATE 8-12-72
APPD
DATE

C
SCALE

102992-12



REVISIONS
DESCRIPTION
* C4, C9, C14 & C19 ARE SELECTED VALUES.
FREQ. RANGE
START
ALT.
(3+4)
(5+6)
ACTUAL
(5+6)
(3+4)
ALT
UL1 COMPARATOR 14585
UL2 COMPARATOR 14585
(STOP)
START FREQ.
FILTER
TO PIN 'L' BD. #3
STOP-FREQ.
O.L.-CH.1
O.L.-CH.2
U.L. CH.1
U.L. CH.2
PRESET GAIN
HOLD
SWEEP VOLT.
RESET/PROG. SWP.
(STOP)
(HOLD) SWP
TO PIN 'L' BD. #4
OUTPUT GND
SELECT
OUTPUT
SWP SPEED RANGE
(X5)
CH.2
J(+15)
T(-15)
J1A (-)
J2A (+)
J3A (+)
J4A (-)
S12
S11
FAST DC REJECT
S8
OFFSET
ZERO
S10
PRESET GAIN
R4 OFFSET
VOLTS F.S.
S5
S7
S6
OUTPUT
J5
PREAMP/OUTPUT AMP
S13
FILTER
OUT
IN
POWER GND
INDICATES OUTPUT
INDICATES INPUT
LEFT CABLE BD.
BAFCO, INC
SCHEMATIC
LEFT CABLE BOARD AND FRONT PANEL
MODEL 916XH
C
SH. 2 OF 3
102992-12



NO	DESCRIPTION	BY	DATE
A	RELEASE		

UNLESS OTHERWISE SPECIFIED
FRACTIONS ±.015
TWO PL. DEC. ±.010
THREE PL. DEC. ±.005
ANGLES ±1/2 DEG.
CUR. PRI. 125 MICROINCH

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BAFCO, INC.

BAFCO, INC

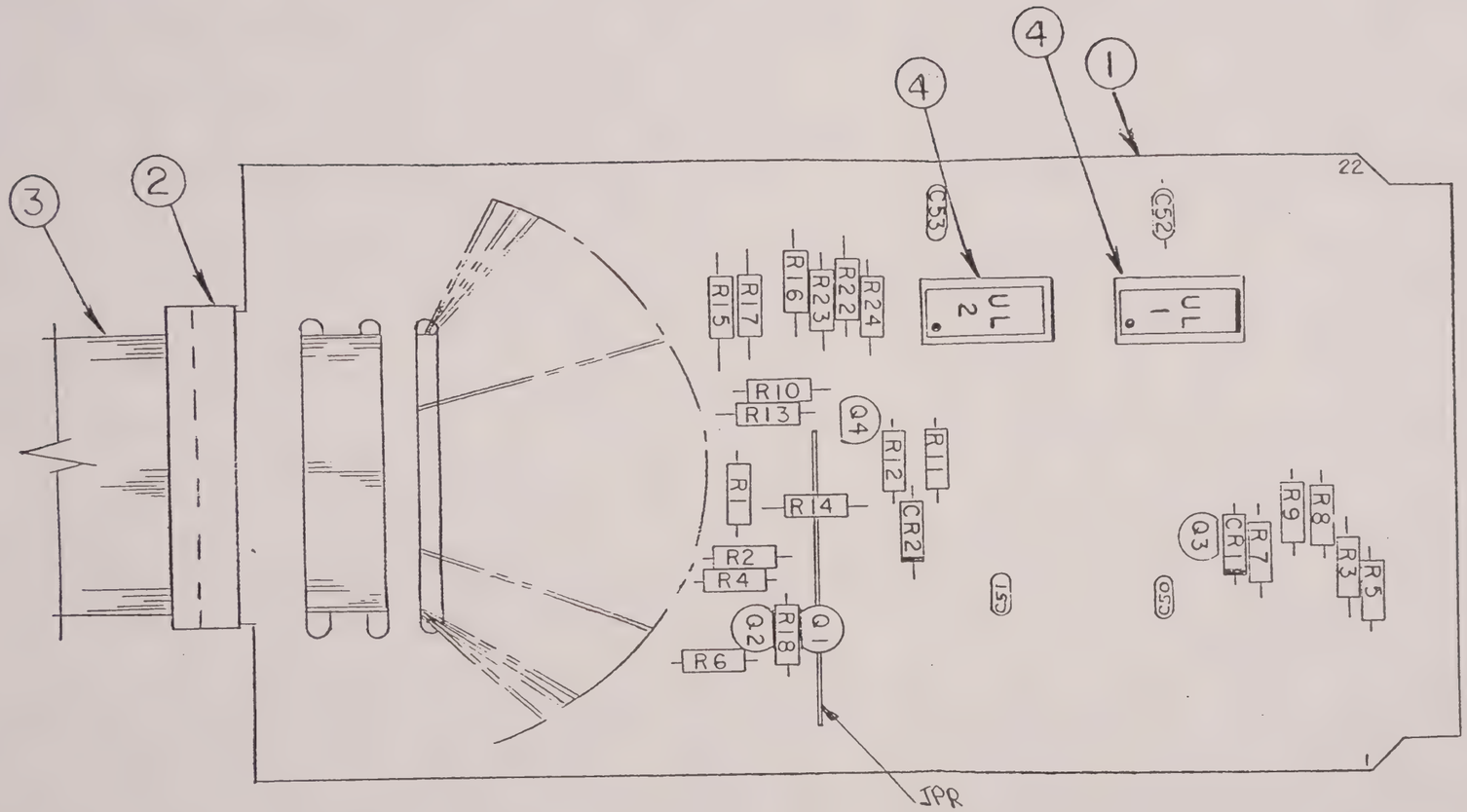
SCHEMATIC
RIGHT CABLE BOARD AND FRONT PANEL
MODEL 916XH

BY Brassi
DATE 9-21-74
APPD
DATE

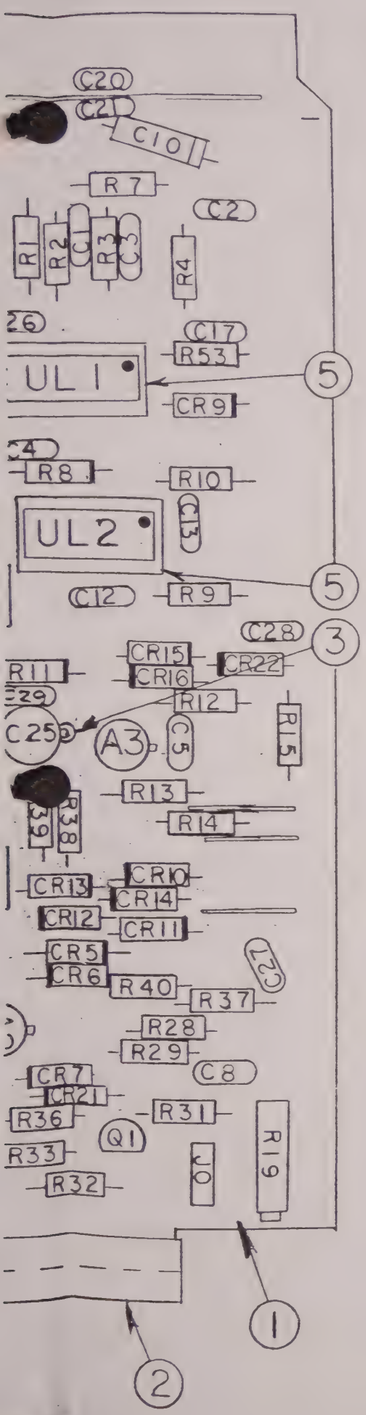
C
SCALE

102992-12
SH. 3 OF 3

REVISIONS			
NO	DESCRIPTION	BY	DATE
A	RELEASE		
B	REV.	AJ	11-22
C	REDRAWN	J.	2-82



UNLESS OTHERWISE SPECIFIED FRACTIONS ± .015 TWO PL. DEC. ± .010 THREE PL. DEC. ± .005 ANGLES ±1/2 DEG. SUR. FIN. 125 MICROINCH	THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	BAFCO, INC	ASSEMBLY LEFT CABLE BOARD P.C. MODEL 916XH	BY DATE APPD DATE	B	SCALE 102993-12



* INDICATES FRONT MOUNTED

C26 .1MF

R53 20Ω — ULI — R54 20Ω — -15

C17 .1M — HEX BUFFER 14050 — C18 .1M

C1 .1MF

M — CH 1 IN — R2 10K — R1 10K — ULI 8 — R7 2K — C2 22PF

L — -15

UL3 D

Y — CH 1 AMP

C3 .1MF

K — CH 2 IN — R3 10K — R4 10K — ULI A — R8 2K — C4 22PF

B — -15

UL3 C

V — CH 2 AMP

C13 10PF — R10 20K — -15

UL2 DUAL ONE SHOT 14528

C12 10PF — R9 20K — -15

UL3 B — ULI D — A — PHASE

UL3 A

C21 .1MFD — C21 .1MFD — C10 .1MFD — 7 H GND — 8 J +15V

C22 .1MFD — C23 .1MFD — C11 .1MFD — 16 T -15V — 17 U GND

UL3 14011 QUAD NAND GATE — 14 — 7 — -15V

+15 — R28 100Ω — C8 .1M

C7 .0022MF 318 — R22 15K — A1 — R23 4.99K — R52 5K — C16 10PF — R19 * 2K

R24 10K — A2 311 — R25 10K — R26 4.99K -15 — C9 .1M

CR5 CR6 CR21 CR7 CR8

R29 20K — R27 1K — R30 20K

R31 200Ω 1/2W — Q1 2N3903 — R32 10Ω — R33 10Ω — Q2 2N3905 — R34 200Ω 1/2W — R35 10Ω

R36 4.7Ω — R40 1.21K

J0 — C27 100PF — R37 2K — ULI F — CR9 — E IN PHASE

CR10 CR11 CR14 CR13 CR12

+15 — R38 5K — -15 — R39 5K

J1 — TO30HZ

CR16 CR15

R11 20K — C29 68PF — C25 SELECT FOR 90°

A3 311 — R14 3.32 — R15 2K — ULI E — D (QUAD)

C28 100 PF

R13 10K — C5 100 PF — R12 20K — CR22

DCSI X

START — +15 — R51 * 10K — -15

R18 20K

J2 — ATTEN. — R55 1K — Z — R56 5K — -15

R45 84.5K — R47 49.9K — R46 499K — R48 2K — C19 .01M — C14 .22MF

R20 3.32K — R41 30.1K — C15 220 PF — R42 24.9K — R44 24.9K

R16 20K — A4 311 — R21 2K — ULI D — Q3 — R43 30.1K — Q4 — A5 312 — R49 4.9K

R17 15K — C24 .01 MFD — R57 15K

W — R50 100K — +15 V — F.R.(5+6)

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BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

ASSEMBLY
SCHEMATIC - P.C. BOARD
7KC TYPE 2
MODEL 916XH REF

C

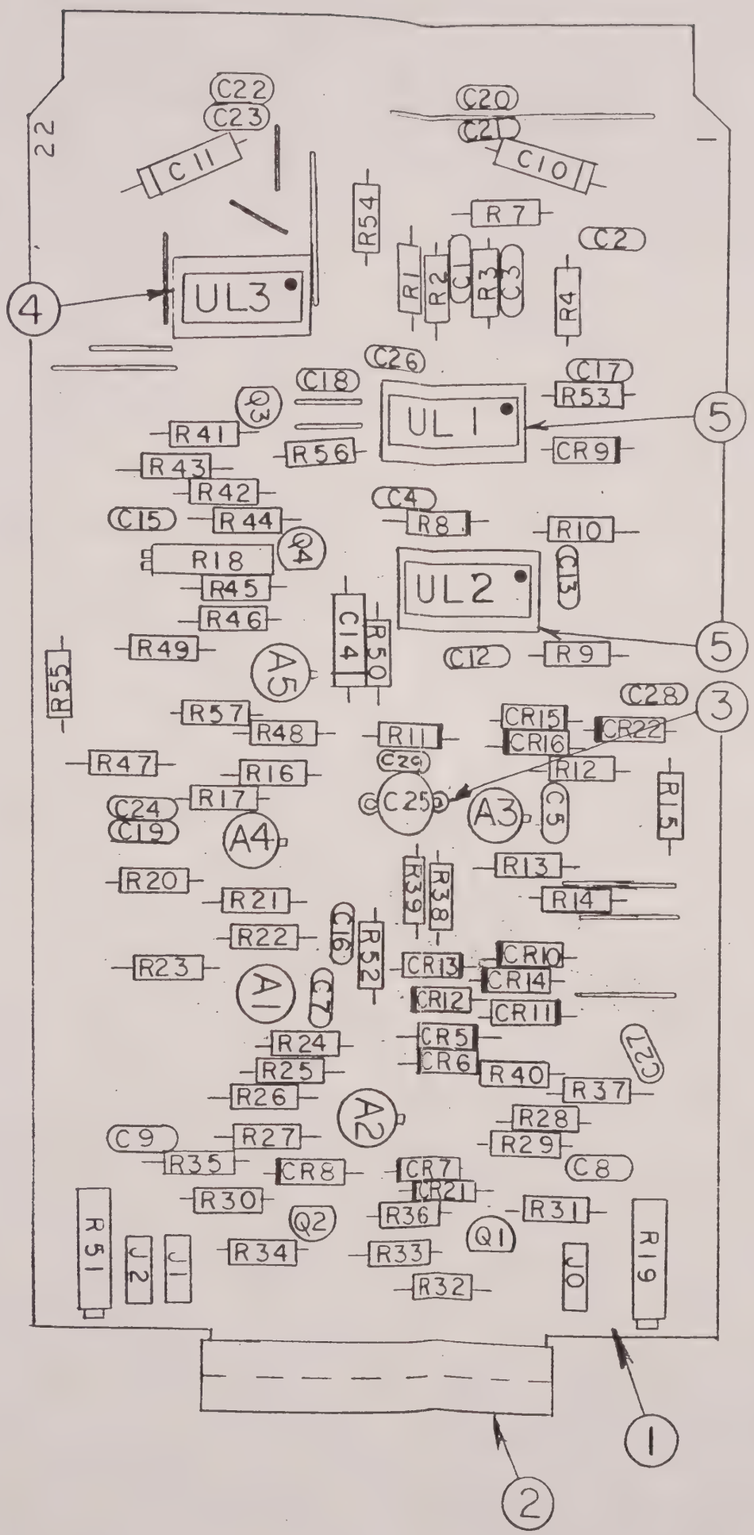
SCALE

103046-12

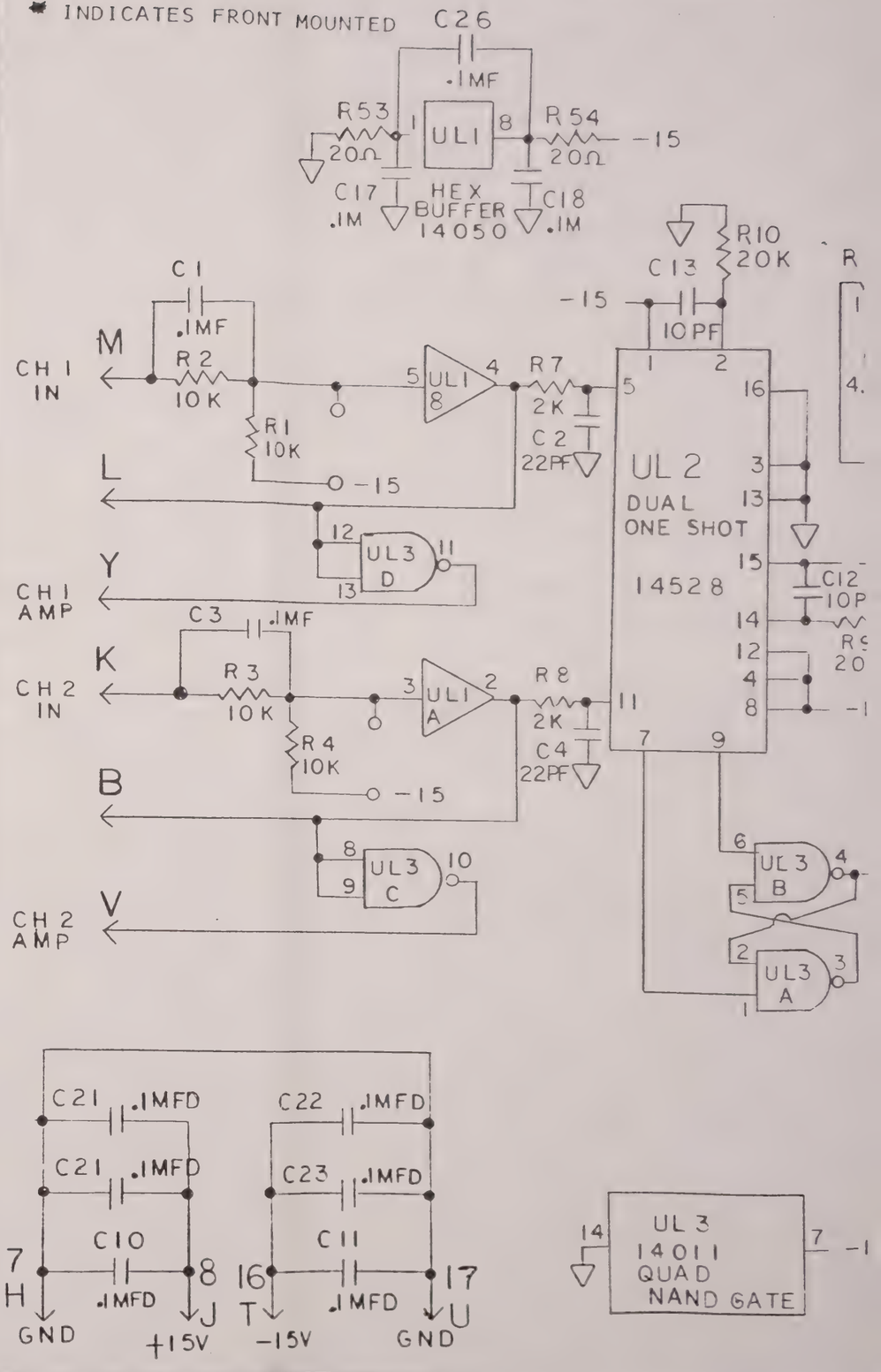
IT	Q	PT NO	DESC	VEND
1	1	103047	P.C. BOARD	
2	1	100073	HANDLE	
3	AR	160-1512-02-05-00	TURRET LUG	CAMBION
4	1	C92-1400	I.C.SOCKET-14	TEXAS
5	2	C92-1600	I.C.SOCKET-16	TEXAS
C10	1		C: .1MF 100 20%	TRW
C11	1	X663F		
C25	1		C: 7-25PF (TRIMMER)	ERIE
CR14	1	IN825	DIODE, ZENER 6V	
Q3	1	TIS-75	TRANS. FET.	TEXAS
Q4	1			
CR21	1	IN5314	DIODE	MOT.
C14	1	X663F	.22MFD	TRW
R31	1		200Ω 1/2W 5%	AB
R34	1		200Ω 1/2W 5%	AB
R36	1		4.72 1/4W 5%	AB

UNLESS OTHERWISE SPECIFIED:

ALL CAPS - ERIE
ALL RESISTORS - CORNING RN60D, 1/4W, 1%
ALL DIODES - FAIRCHILD FD6666
ALL TRANSISTORS - MOTOROLA
ALL I.C.'S - MOTOROLA



* INDICATES FRONT MOUNTED



NO	REVISIONS	
B	REDRAWN 2/82	
A	RELEASE 9/74	AG

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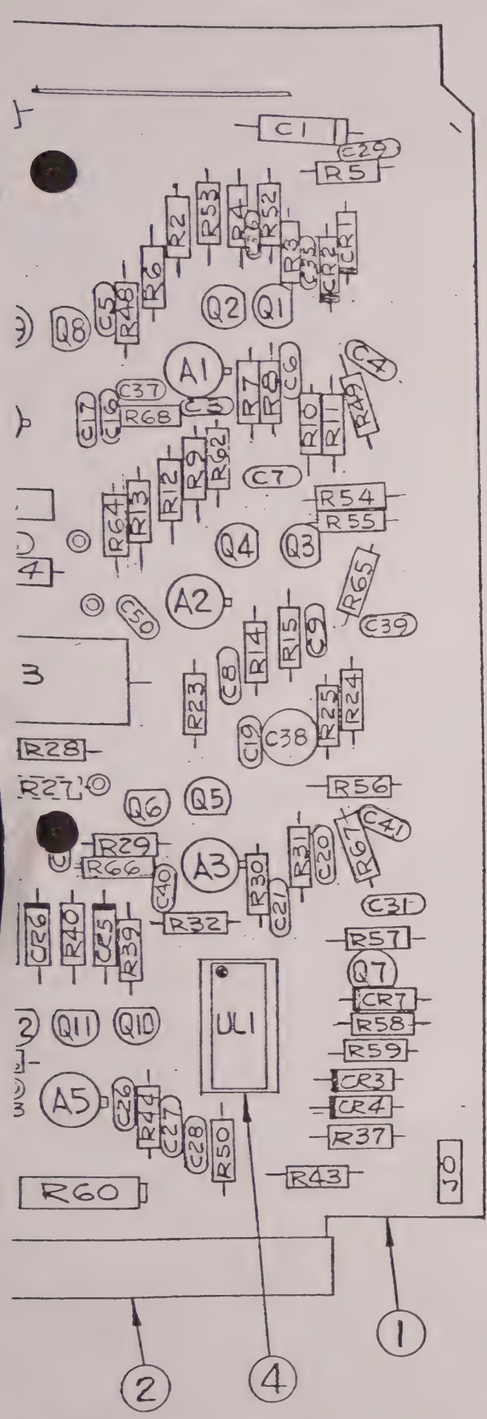
BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE



SELECTED CAPS.
.25% PRECISION RES.
RES LOAD FOR 916H ONLY.

-15 R66 100Ω C40 .1MF A3, PIN 4

+15 R67 100Ω C41 .1MF A3, PIN 7

+15 R49 49.9Ω C4 .1MF A1, PIN 7

-15 R48 49.9Ω C5, .1MF A1, PIN 4

-15 R64 100Ω C50 .1MF A2, PIN 4

+15 R65 100Ω C39 .1MF A2, PIN 7

H, 7 GND

J, 8 +15

T, 16 -15

U, 17 GND

C31 .1MF C29 .1MF C1 .1MF

C32 .1MF C30 .1MF C2 .1MF

L INPUT

* R2 30.1K

C35 2.2PF

*R3 30.1K

R52 30.1K

R4* 10K

C36 2.2PF

R53 10K

C6 4.7PF

*R8 30.1K

R7 5K

C3 4.7PF

A1 318

R6 10K

R68 392K C37 2.2PF

R62 200K

R55 20K

Q3

*R9 121K

⊗R10 C7⊗

*R11 8.06K 22 PF

R54 8.06K

Q4

C9 2.2PF

*R15 121K

*R23 121K

R14 5K C8 4.7 PF

A2 318

R13 50K

R12 121K

C38 7-25

⊗R25 20K C19 ⊗

*R24 8.06K 22 PF

R56 8.06K

Q5

Q6

C20 2.2PF

*R31 121K

R30 5K C21 4.7 PF

A3 318

R29 50K

R32 20Ω → 21

R51 200Ω J1

CR1

CR2

R5 40.2K

C34 SEL

△C13 5.2MF

Q8 → P (F.R. 1+2)

C15, SEL

C14 .052MF

Q9 → R (F.R. 1+2+3+4)

C16 470PF

C17

C18 100PF

R26 5K

R27 (301Ω) SEL

R21 2M

R22 221K

R28 45.3K

R38 40.2K

C33 .01MF

A4

R18 10K

R19 100K

Q14

CR5

CR6

-15V

MAX. GAIN C

R57 10K

Q7

CR7

R59 10K

R58 40.2K

+15

R37 40.2K

CR3

CR4

S (ALT F.R.)

CR8 6V CR9 -15

Q10

*R39 165K

Q11

*R40 82.5K

Q12

*R41 41.2K

R63 CAL

Q13

*R42 20.5K

R50 20Ω

C28, .01MF

R43 20K

C27, .01MF

R44 12.4K R60, 5K

C26 33PF

A5 308

22 (db)

J2

R45 5K

J0

R46 (1) 10K -15

R47 100Ω

GAIN

14050 ULI HEX BUFFER

A — X2

B — X4

4 — X16

3 — X256

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BAFCO, INC.

BAFCO, INC

BY Grassi
DATE 3-11-75
APPD
DATE

ASSEMBLY BD·3 & 4
SCHEMATIC - P.C. BOARD
INPUT AMPLIFIER
MODEL 916XH REF

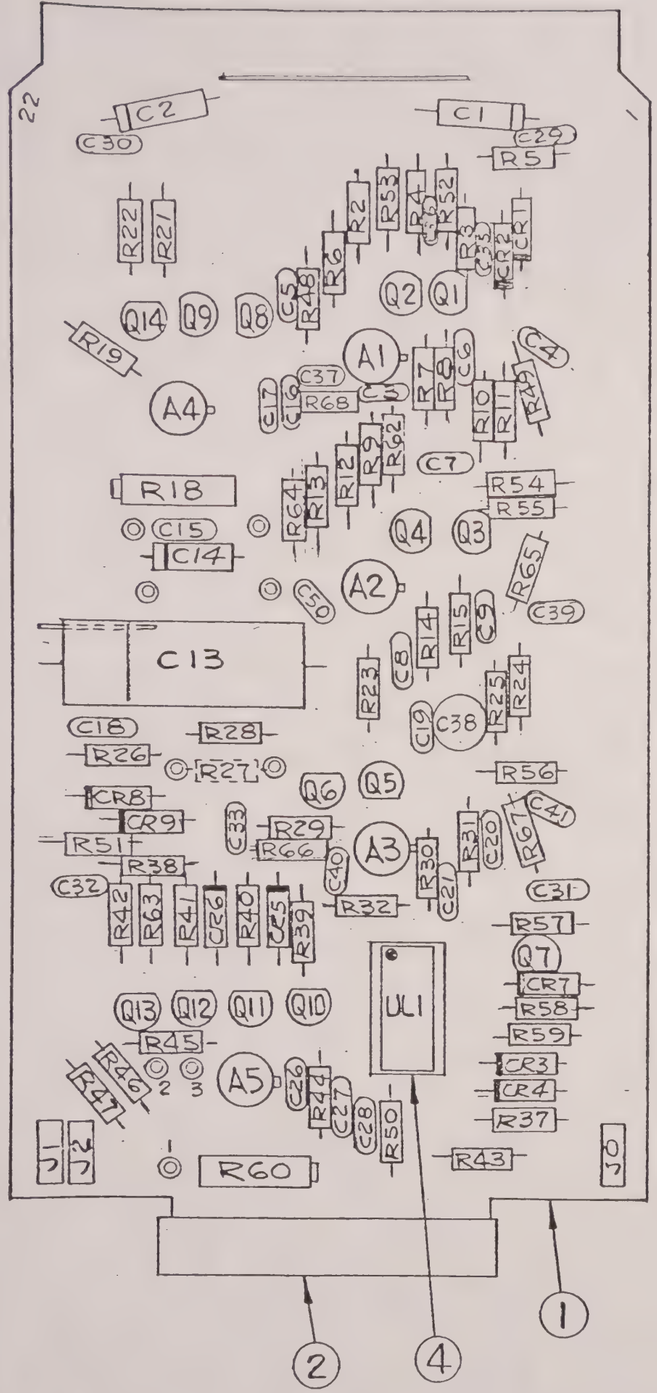
C

SCALE ——

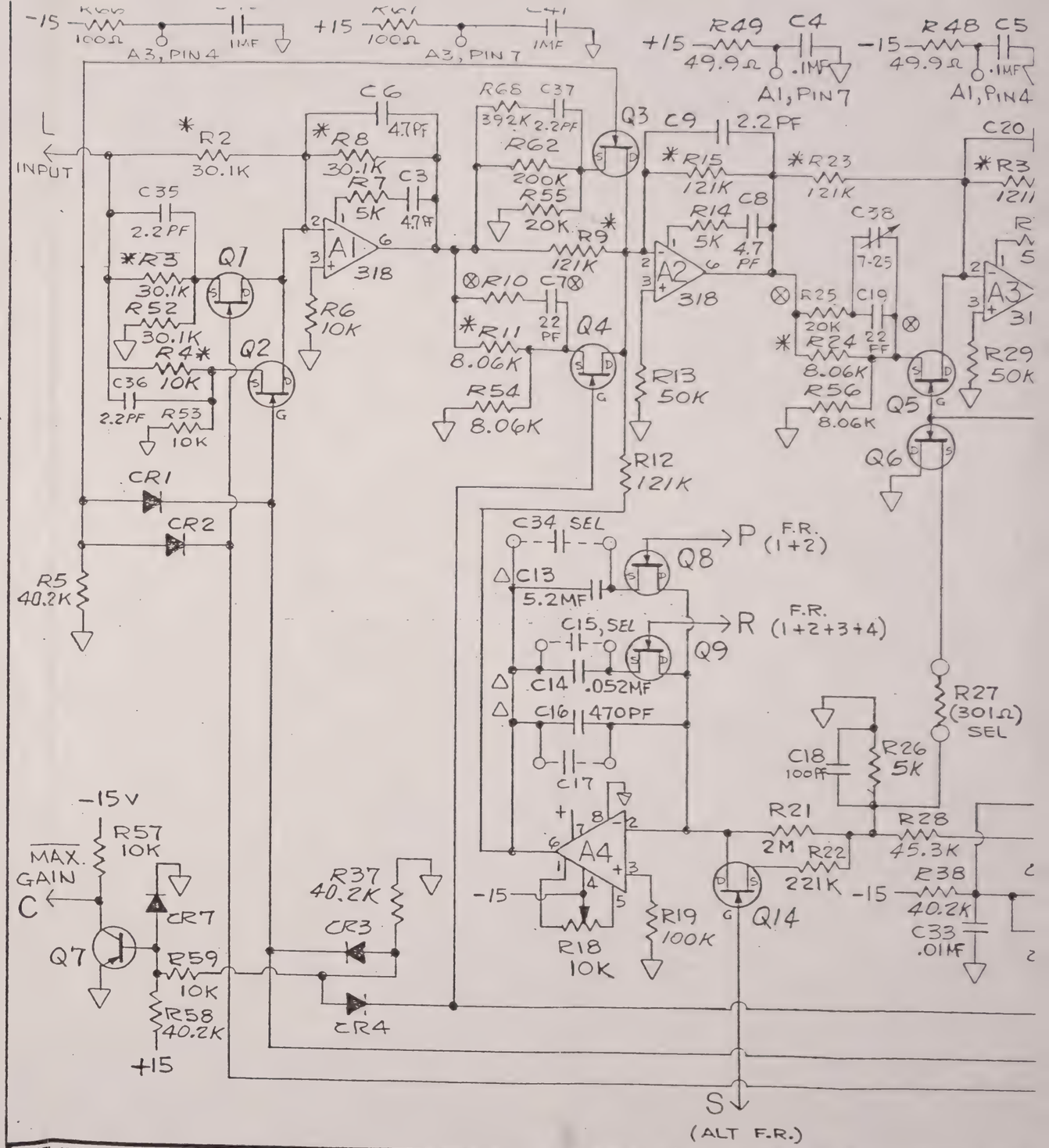
103110-12

1	103084	P.C. BOARD	BAFCO
1	100073	HANDLE	"
AR	160-1512-02-05-00	TERMINAL	CAMBION
1	92-1600	I.C. SOCKET	TEXAS
[illegible]	M-270	EYELET	MARK
1	X663F	.1MF 100V 10%	↑
1	X463UW	5MF 100V 10%	TRW
1		.05MF 100 10%	↓
1	LM 318	AMPLIFIER	NAT'L.
1	LM 308	AMPLIFIER	NAT'L.
1	3522J	AMPLIFIER	BURR/BRN
1	1N5314	DIODE 6V.	MOT.
1	1N825	DIODE, ZENER	MOT.
1	2N3905	TRANSISTOR-NPN	MOT.
1	14050	I.C. 16 PIN	MOT.
			CORNING
			"

NOTES:
- UNLESS OTHERWISE SPECIFIED:
  - ALL CAPS — ERIE
  - ALL RESISTORS - 1/4W, 1% RN60D — CORNING.
  - ALL DIODES - FD6666 — FAIRCHILD
  - ALL TRANSISTORS - U1899E (SILICONIX)



△ INDICATES SELECTED CAPS.
✱ INDICATES .25% PRECISION RES.
⊗ INDICATES LOAD FOR 916H ONLY.



REV.	C35 ADD TO P.C. C36 ASSY. 8-82
RELEASE	

REVISIONS

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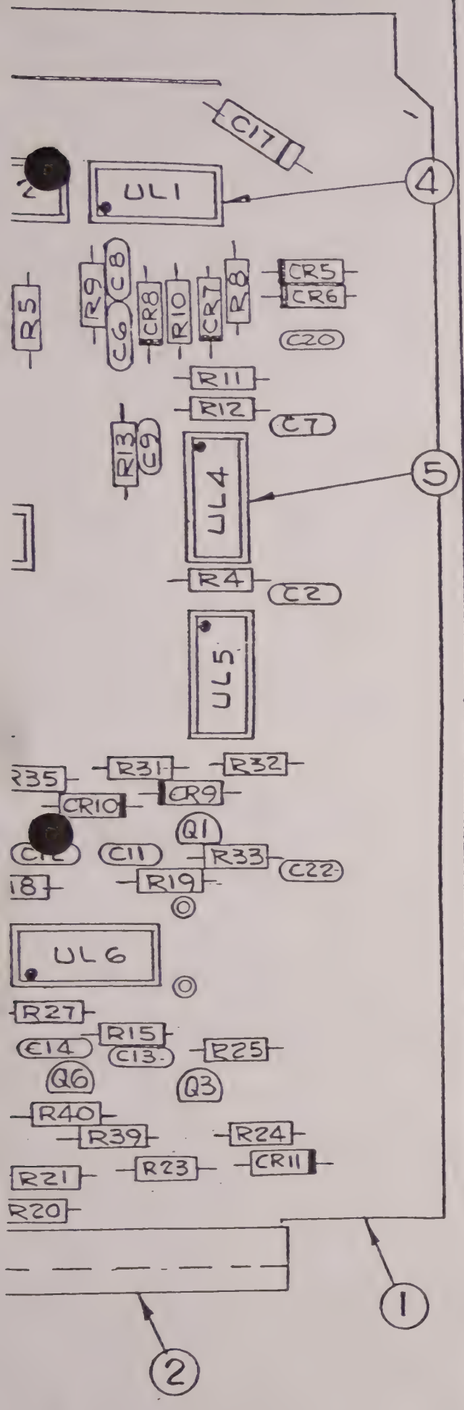
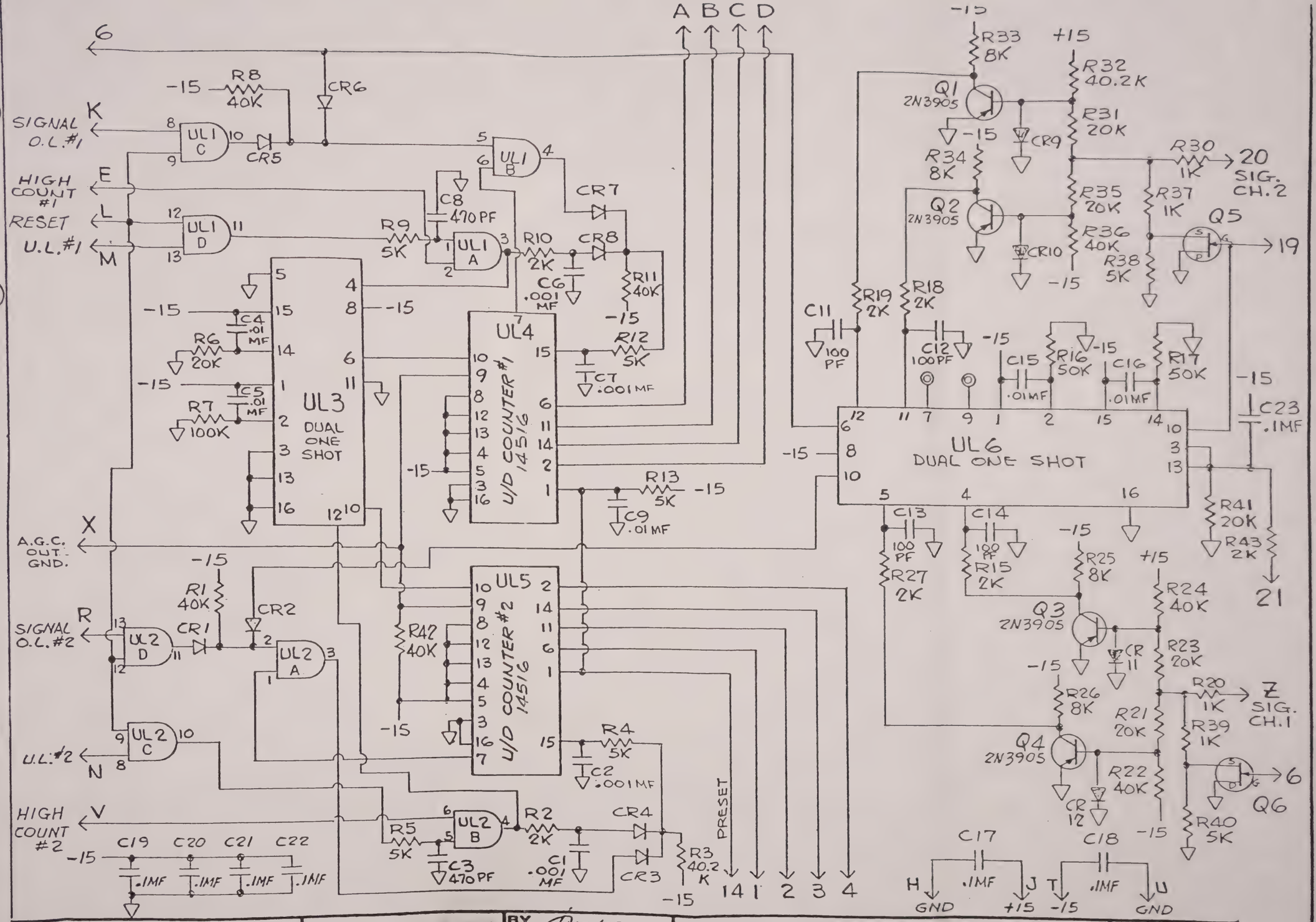
BAFCO, INC.

BAFCO, INC

BY Grassi
DATE 3-11-75
APPD
DATE

AS
SCHEMATIC
INPUT AMP
MODEL 916XH





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BAFCO, INC.

BAFCO, INC

BY BIASSI
DATE 11-15-74
APPD
DATE

ASSEMBLY #5
SCHEMATIC - P.C. BOARD
A.G.C. LOGIC - 2 CHANNEL
MODEL REF

C SCALE FULL

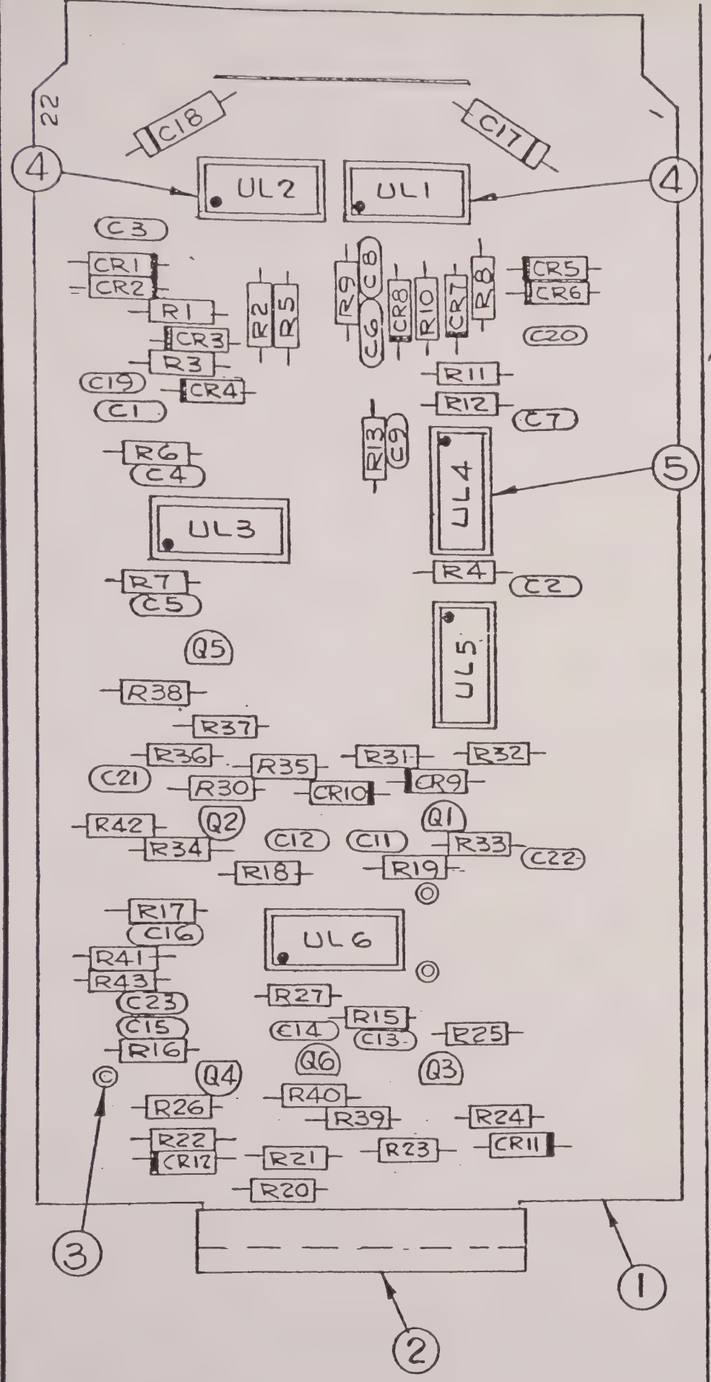
103116

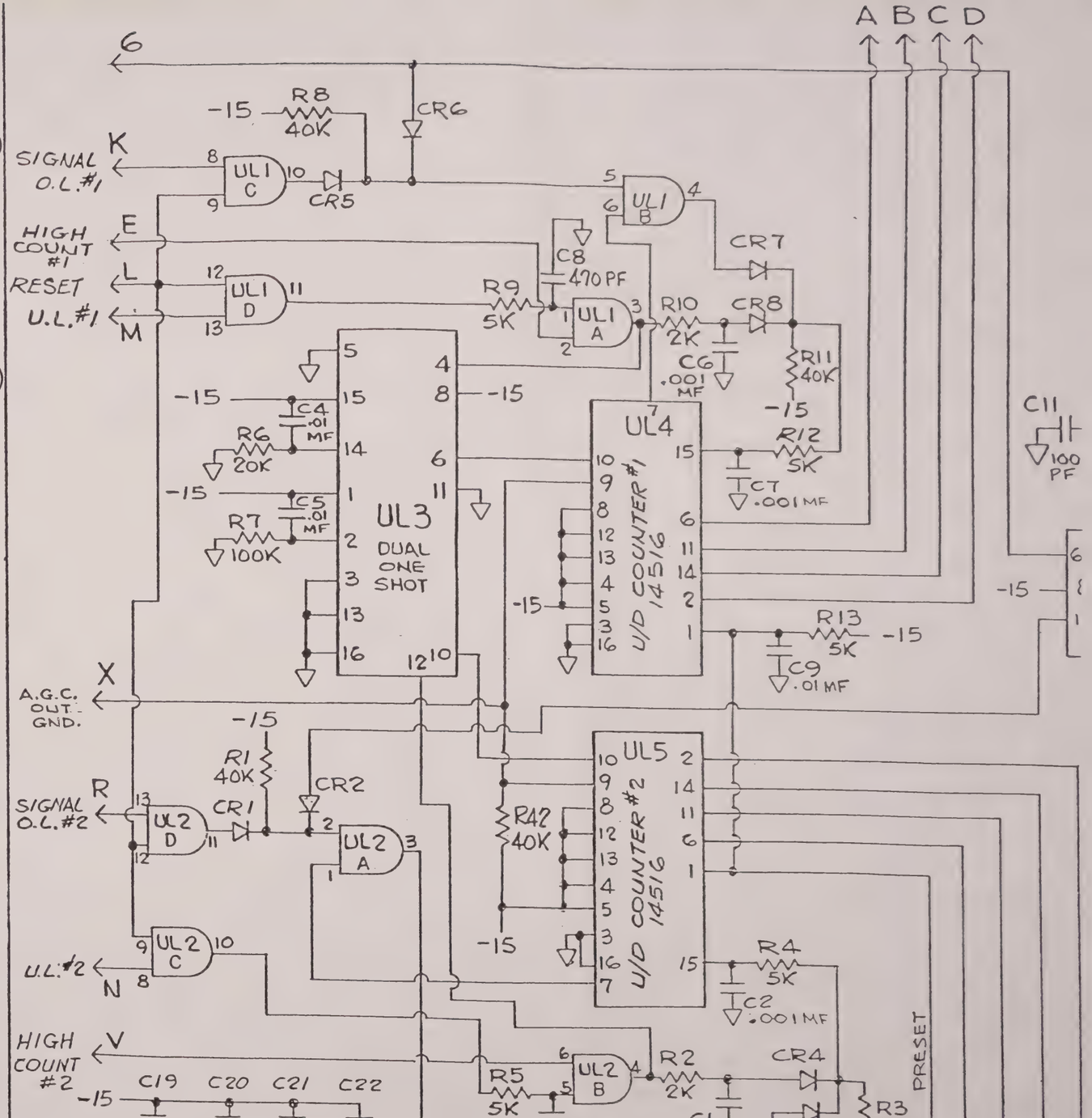
103117	P.C. BOARD	
100073	HANDLE	
160-1512 02-05-00	TERMINAL	CAMBION
C[illegible]400	I.C. SOCKET	TEXAS
[illegible]-1600	I.C. "	"
[illegible]-270	EYELET	MARK
X663F	C: .1MFD 100V 20%	TRW
T1S-75	TRANSISTOR-FET	MOT. "
7424	I.C. MC14081	MOT
7502	I.C. MC14528	MOT
7320	I.C. MC14516	MOT

TES:
UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS - ERIE
ALL RESISTORS - 1/4W, 1%
RN60D - CORNING.
ALL TRANSISTORS - MOTOROLA
ALL I.C.'S - MOTOROLA
ALL DIODES - FD6666, FAIRCHILD.

REV. R43 ADD	6-77
REV. 3-76	
REV [illegible]-75	
REV 10-75	H
REV. 6-75	
RELEASE	

REVISIONS





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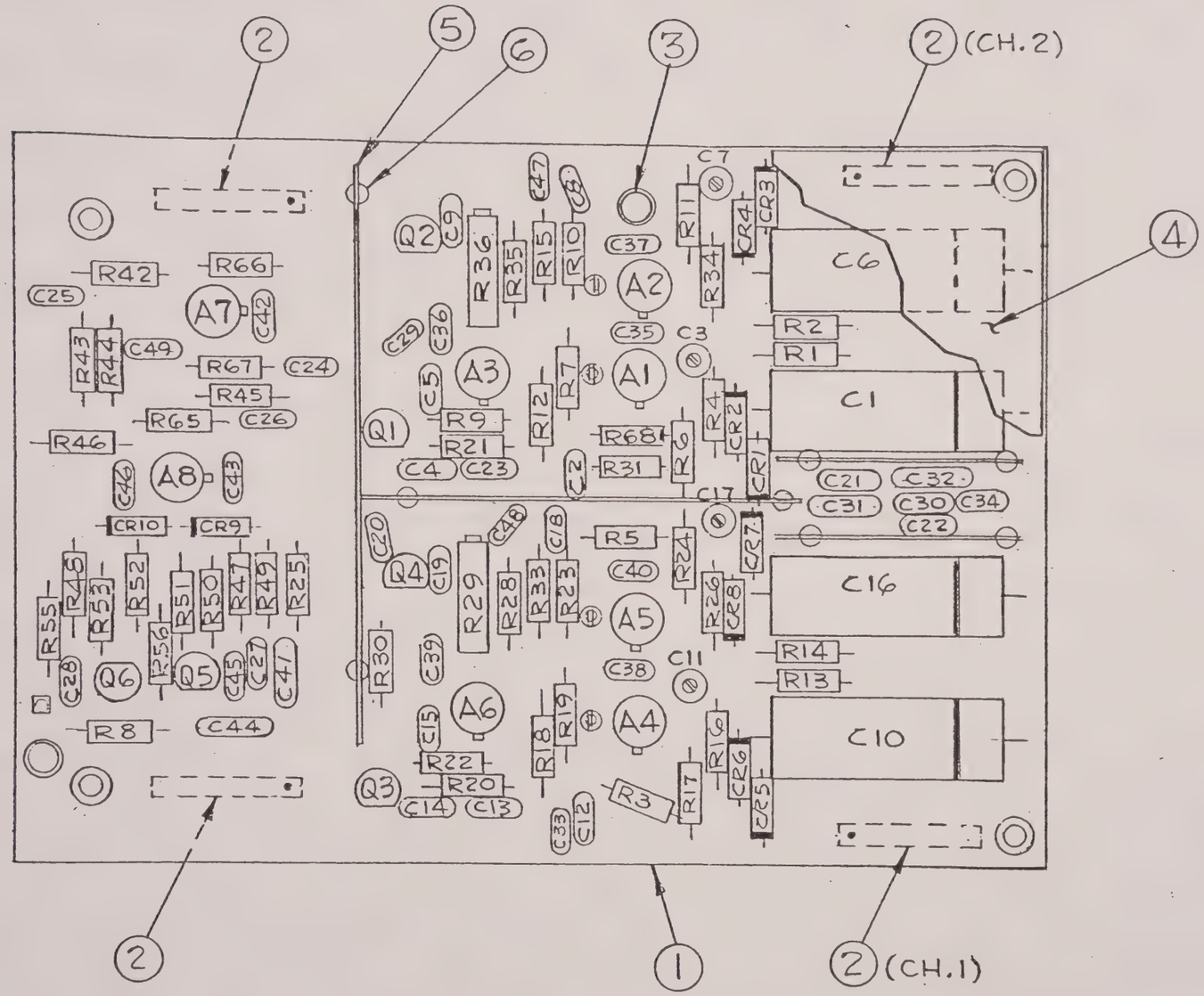
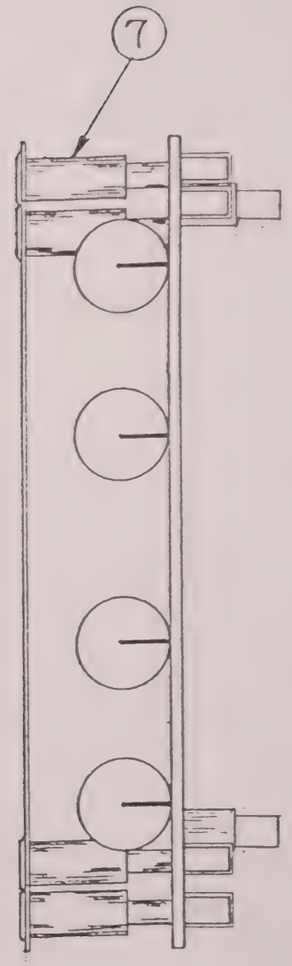
BAFCO, INC.

BAFCO, INC

BY [illegible]
DATE 11-15-74
APPD
DATE

AS
SCHEMATI
A.G.C. LOG
MODEL





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BAFCO, INC.

BAFCO, INC

BY GRASSI
DATE 4-18-75
APPD
DATE

ASSEMBLY
INPUT/OUTPUT AMPLIFIER BD.
MODEL 916H REF

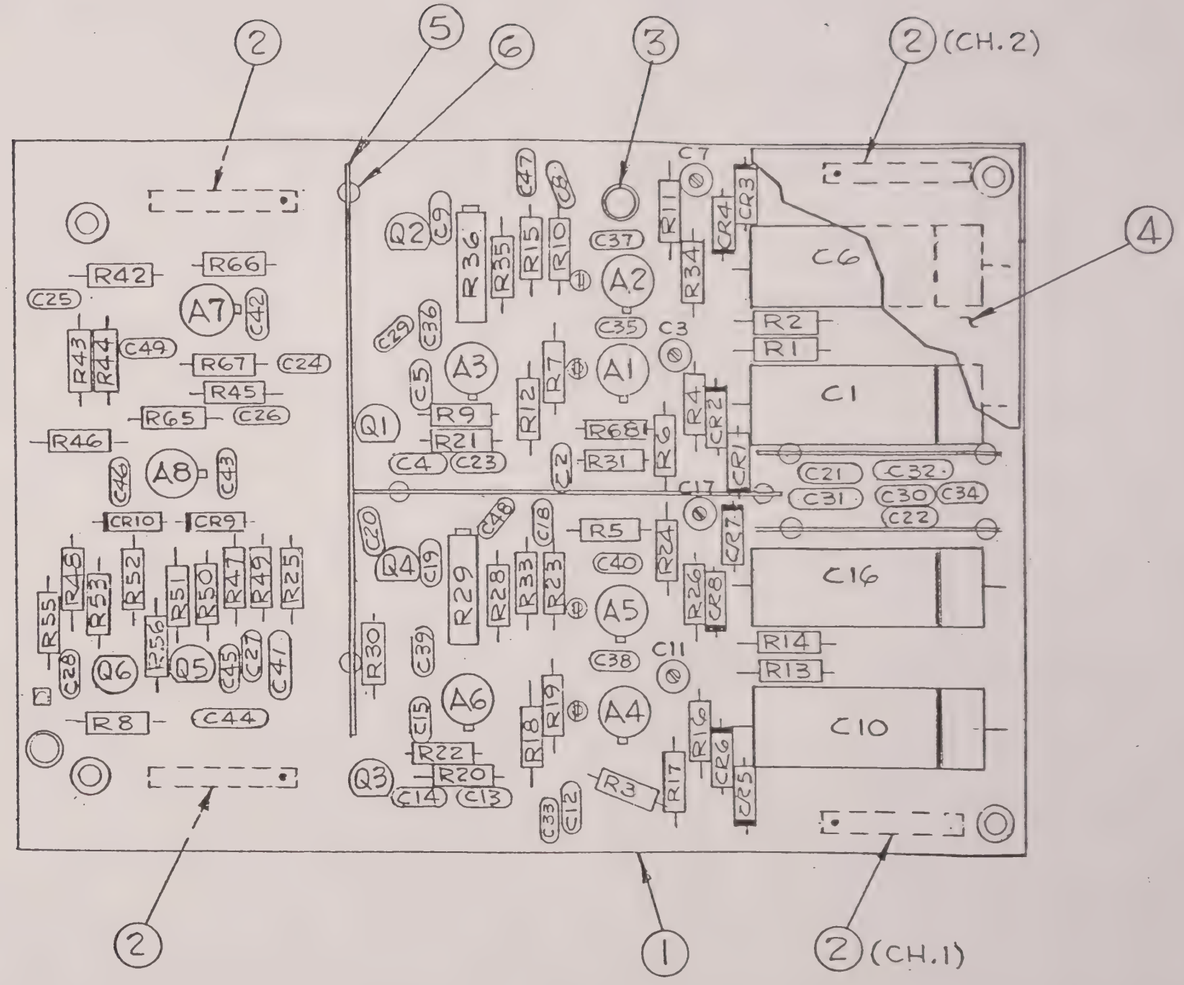
C | SCALE FULL

103273-5

T	Q	PT NO	DESC	VEND
	1	103031	P.C. BOARD	
	4	8129-005 612-002	P.C. COMN	ELCO
		100045A	SPACER	BAFCO
		103030	SHIELD BD.	"
4 6, 11, 16 17 24 26	1	CC2004F	RES. 2MEG.	AB
T	1			
6 10 16	1	X463UW	5MF 10% 100V	TRW
A1	1	LM310	AMPLIFIER	NAT'L.
A2	1	LM310	↕	↕
A3	1	LM318		
A4	1	LM310		
A5	1	LM310		
A6	1	LM318		
A7	1	LM310		
A8	1	LM318	AMPLIFIER	NAT'L.
R[illegible]	1			
R[illegible]	1			
R[illegible]	1			
CR4	1	IN4114	DIODE, ZENER	MOT.
CR5	1			
CR6	1			
CR7	1			
CR8	1			
R29	1	89PR	1K VAR. POT.	BECKMAN
R36	1			
Q5	1	2N3903	TRANSISTOR	MOT.
Q6	1	2N3905	"	"
R50	1		R: 100Ω ½W 5%	AB
R53	1		R: 100Ω ½W 5%	AB
R56	1		R: 4.7Ω ¼W 5%	AB

1-UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS 1/4W, 1%
RNC60D - CORNING.
ALL CAPS - ERIE
ALL DIODES - FD6666 - FAIRCHILD
ALL FETS - U1899E SILICONEX

NO	REVISIONS		
D	REV. R68 ADD 8-76	G	REV. DELETE R75,76,77,78 6/81
C	REV 3-76	F	REV. R75,76-77,78 WAS 69,70,71,72
B	REV. 11-75	E	REV. R70,71,72,73 ADD 5-77
A	RELEASE		



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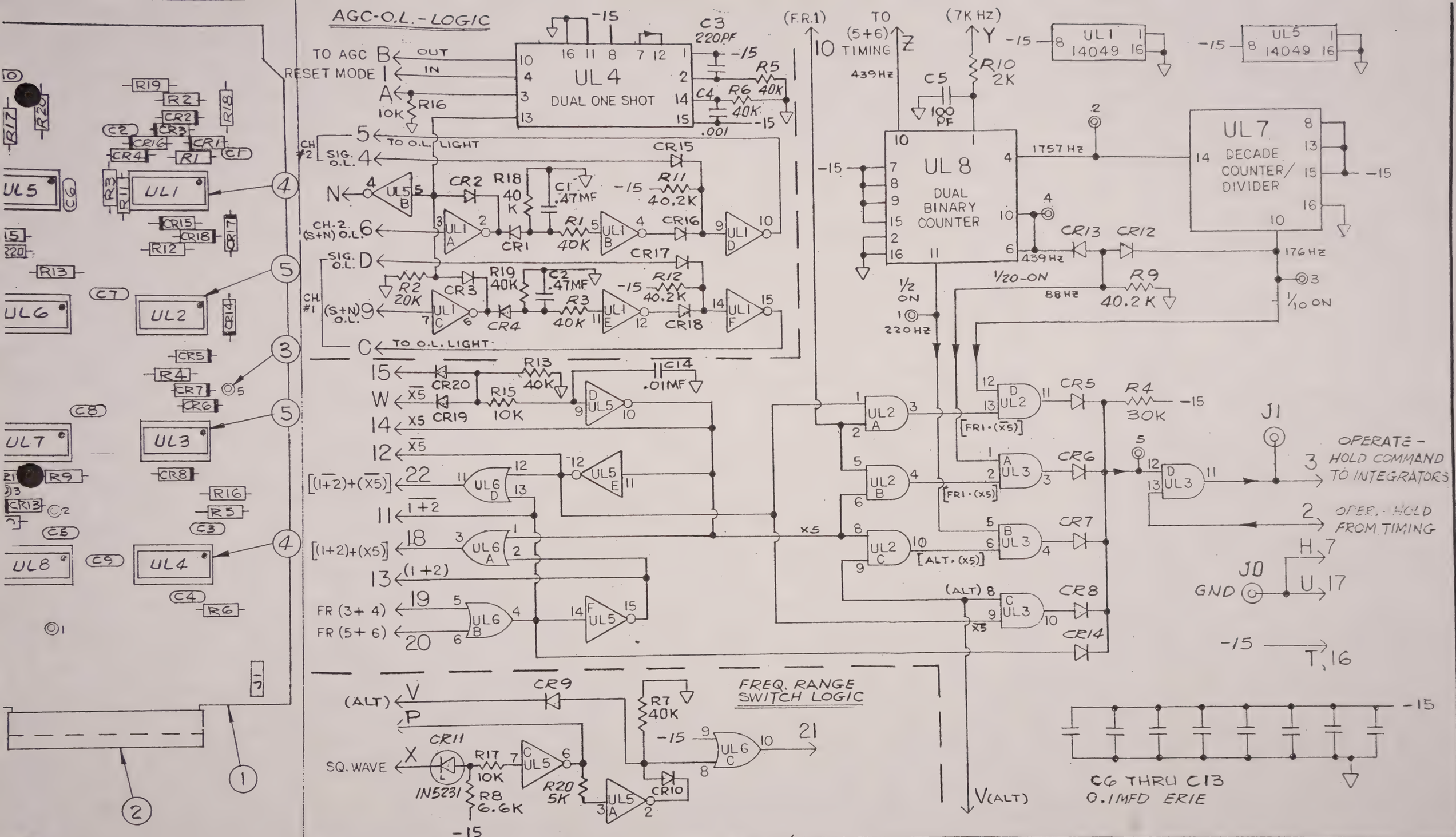
BAFCO, INC.

BAFCO, INC

BY GRASSI
DATE 4-18-75
APPD
DATE

A
INPUT/OU
MODEL 916H



THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING.
BAFCO, INC.

BAFCO, INC

BY BRASSI
DATE 6-6-75
APPD
DATE

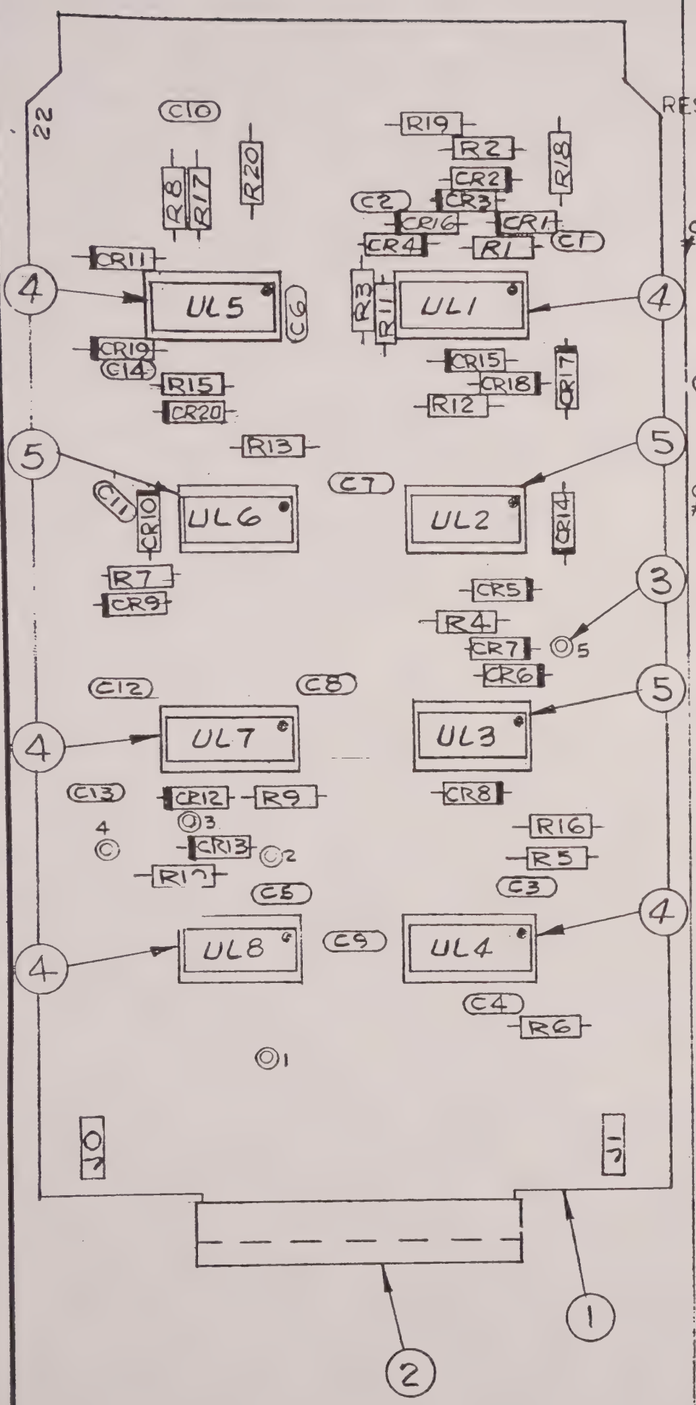
ASSEMBLY #11
SCHEMATIC - P.C. BOARD - X5 INTEGRATE
MODEL 916 REF

C
SCALE FULL
103306-1

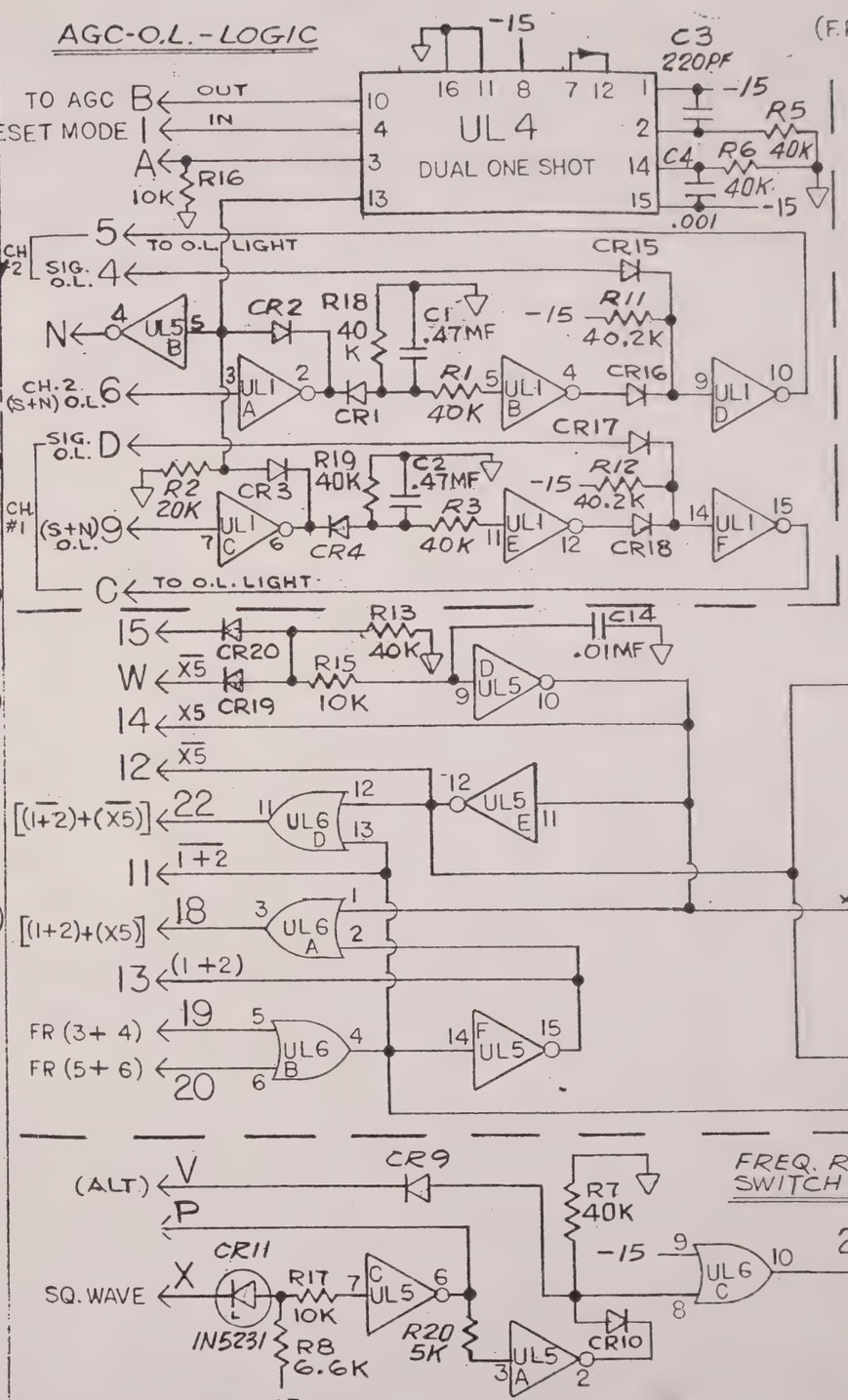
IT	Q	PT NO	DESC	VEND
1	1	103307	P.C. BOARD	BAFCO
2	1	100073	HANDLE	
3	2	160-SPC-02.05.00	TURRET LUG	ZAMBION
4	2	516-AG-11D	I.C. SOCKET	VECTOR
5	3	514-AG-11D	I.C. SOCKET	VECTOR
UL1	1	14049	I.C. 16 PIN	MOTOROLA
UL2	1	14081	I.C. 14 PIN	
UL3	1	14081	I.C. 14 PIN	
UL4	1	14528	I.C. 16 PIN	
UL5	1	14049	I.C. 16 PIN	
UL6	1	14071	I.C. 14 PIN	
UL7	1	14017	I.C. 16 PIN	
UL8	1	14520	I.C. 16 PIN	MOTOROLA
CR11	1	1N5231	DIODE, ZENER	MOTOROLA

NOTES:
1--UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS RN60D,
1/4 W. 1% - CORNING
2-ALL DIODES FD6666 -
FAIRCHILD
3-ALL JACKS #430 H.H. SMITH

NO	REVISIONS
F	REV 6-76
E	REV. 12-16-75
D	REV 11-21-75
C	REV 11-75
B	REV 6-75
A	RELEASE



AGC-O.L.-LOGIC



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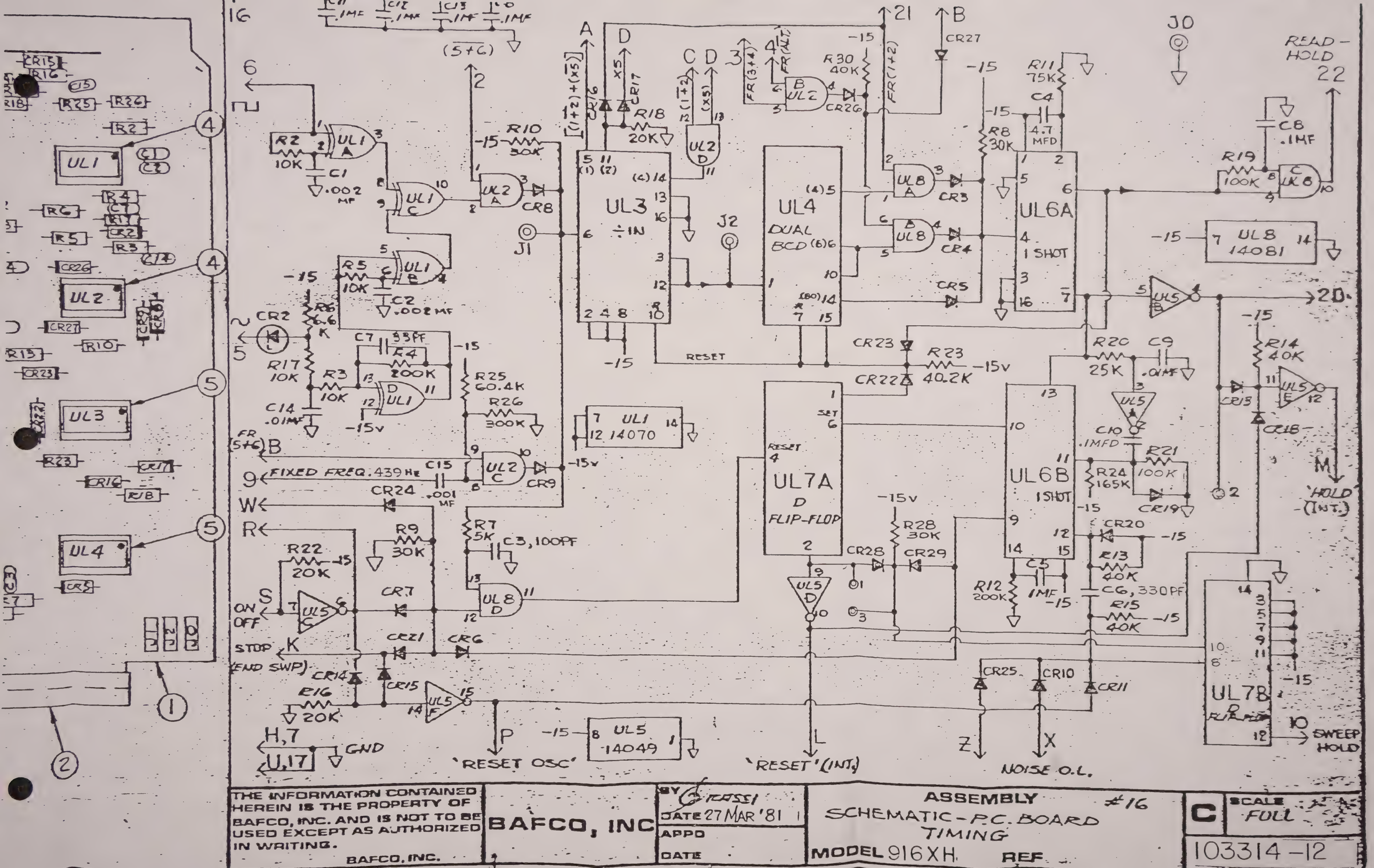
BY BRASSI DATE 6-6-75	SCHEMATIC - X5 INT
APPD DATE	MODEL 916



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BAFCO, INC.

BAFCO, INC

BY [illegible]
DATE 27 MAR '81
APPD
DATE

ASSEMBLY #16
SCHEMATIC - P.C. BOARD TIMING
MODEL 916XH REF

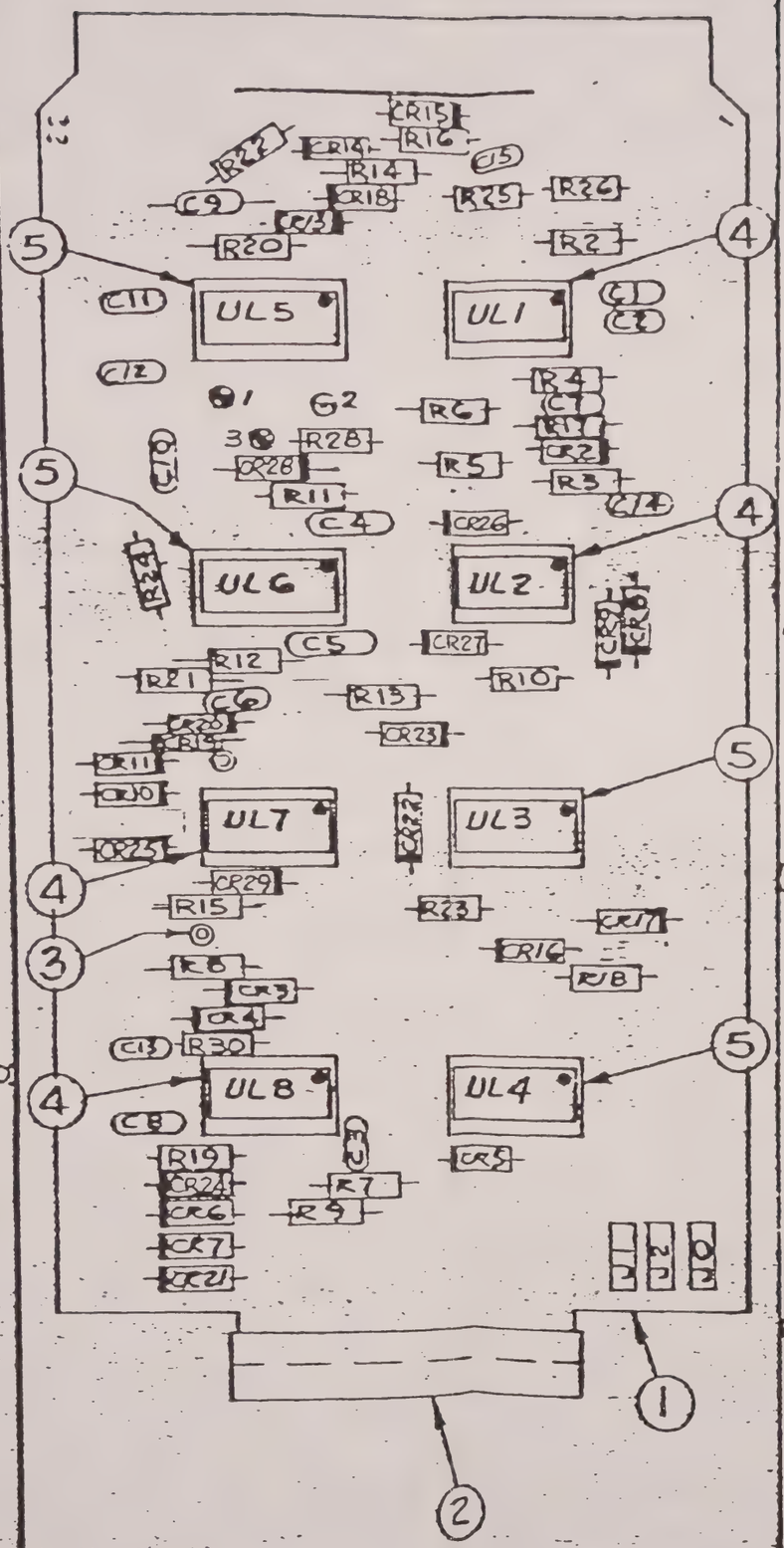
C SCALE FULL

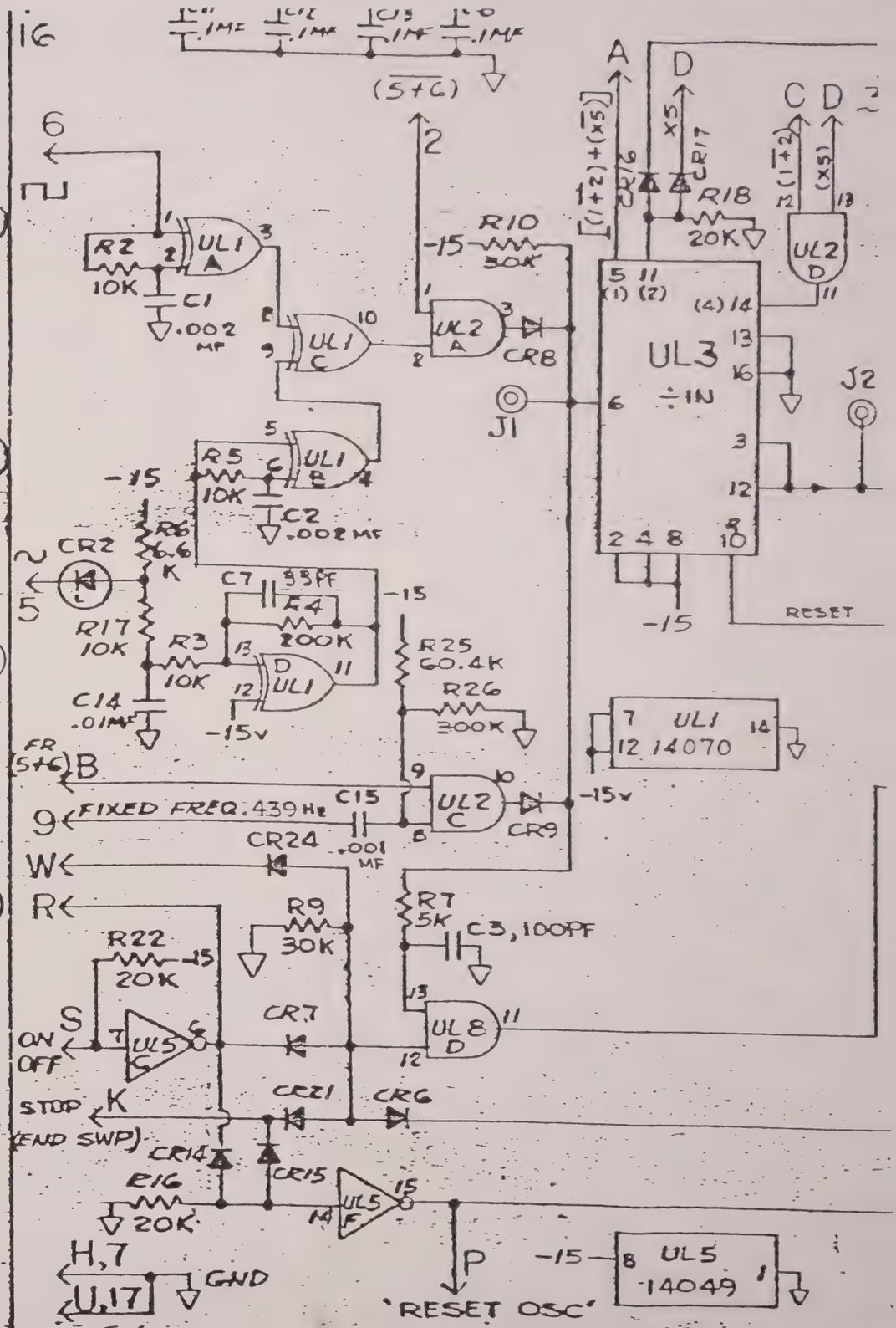
103314-12

1	1	103315	P.C. BOARD	BAFCO
2	1	100073	HANDLE	
3	AR.	460-1512-02-00-00	TURRET LUG	ZAMBION
4	4	514-AG-11D	I.C. SOCKET	AUGAT
5	4	516-AG-11D	I.C. SOCKET	"
UL1	1	14070	I.C. 14 PIN	MOT.
UL2	1	14081	14	
UL3	1	14522	16	
UL4	1	14518	16	
UL5	1	14049	16	
UL6	1	14528BE	16	
UL7	1	14013	14	
UL8	1	14081	I.C. 14 PIN	MOT.
CR2	1	IN825	DIODE-ZENER	"
C1	1		.002	ERIE
C2	1		.002	
C3	1		33PF	
C9	1		.01MFD	
C10	1		.01MFD	
C4	1		1MFD .50V	
C5	1		1MFD, 100V	ERIE
C3	1		100PF	"
C6	1		150PF	

NOTES:
1- UNLESS OTHERWISE SPECIFIED
ALL CAPACITORS - ERIE
ALL DIODES - FD6666 F'CHILD.
ALL RESISTORS - 1/4W, 1%
RNC60D - CORNING
ALL JACKS - #430 A.L. SMITH

C	REV. UL7, 8 & 10 ADD, 7-82
B	REV. PIN 9 WAS 220Hz
A	RELEASE
	REVISIONS





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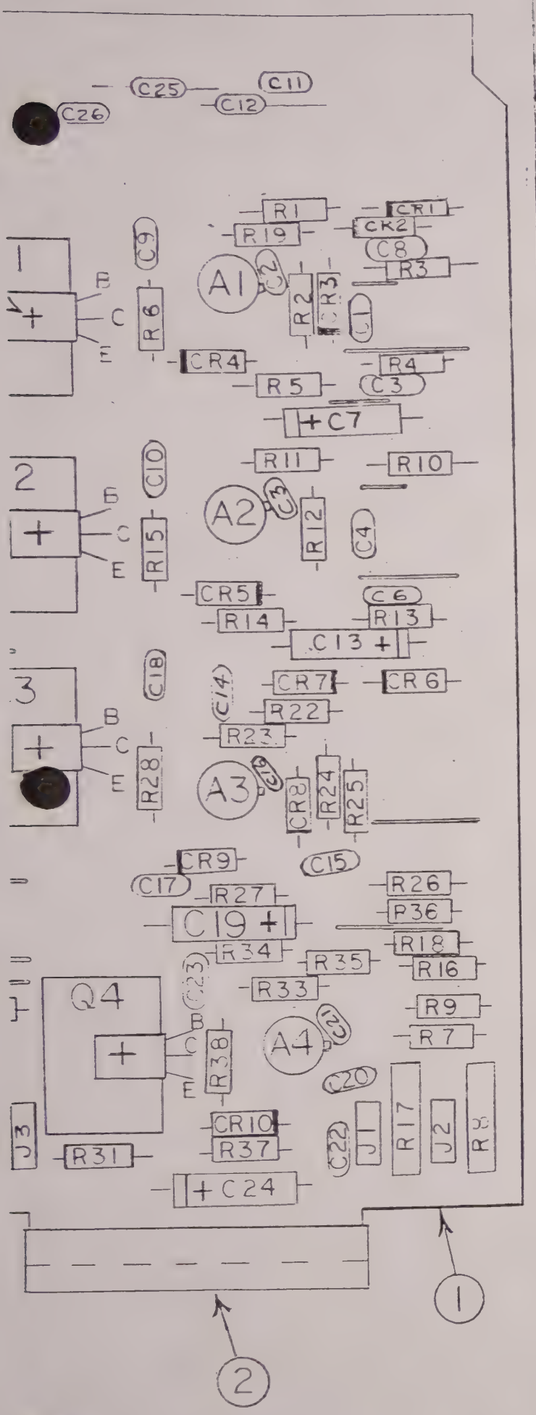
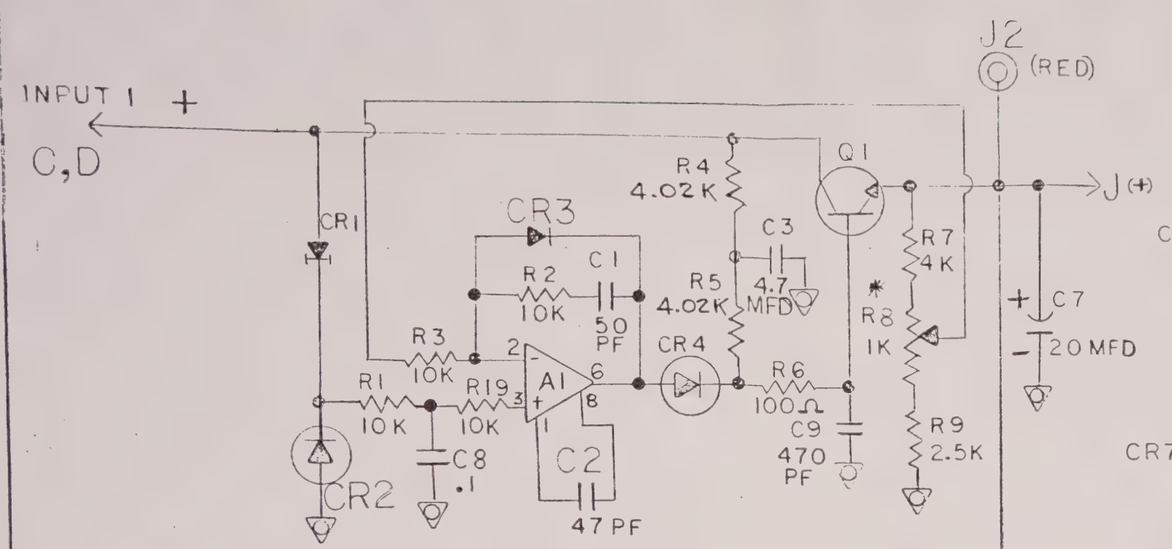
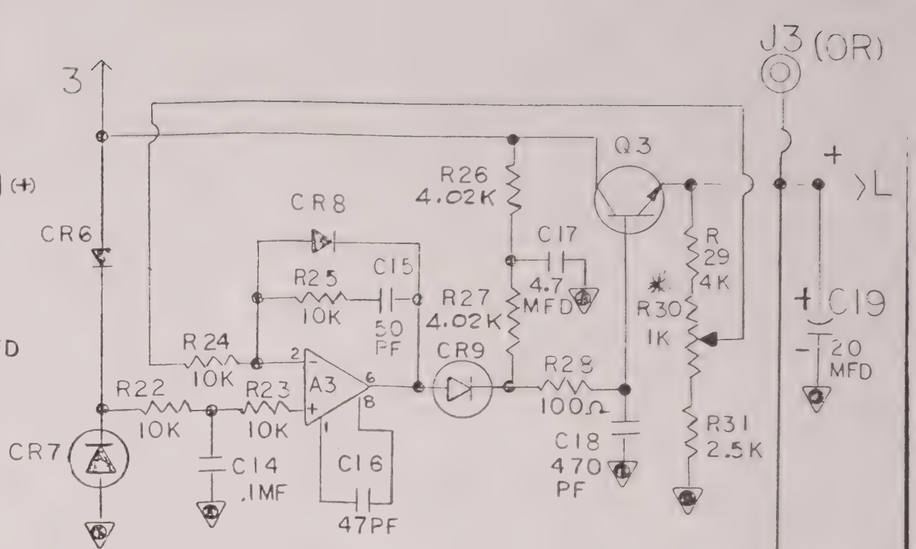
BAFCO, INC.

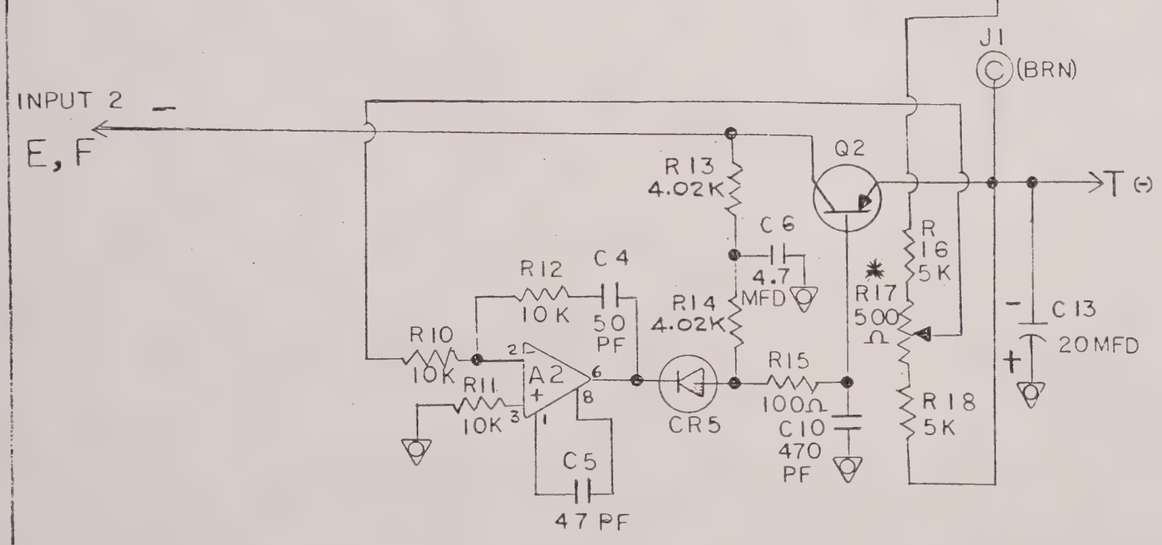
BAFCO, INC

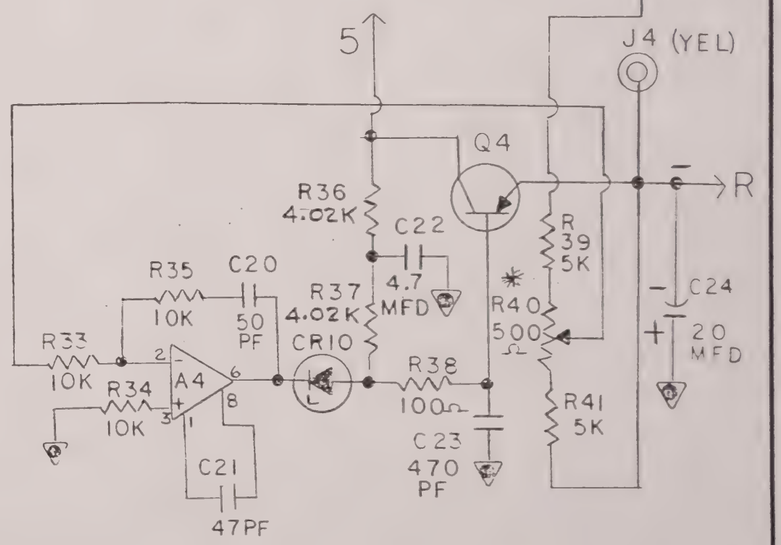
BY
DATE 27 MA
APPD
DATE

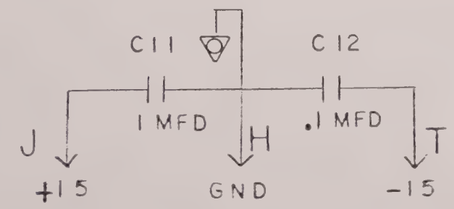


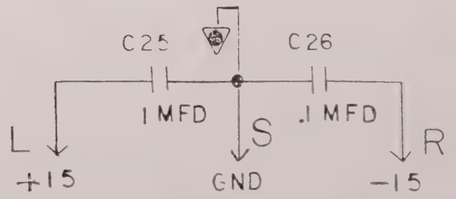












*INDICATES FRONT OF P.C. BD. MTG.

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BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

ASSEMBLY #18
SCHEMATIC - P.C. BOARD
MULTIPLE REGULATOR
MODEL 916H/916XH **REF**

C

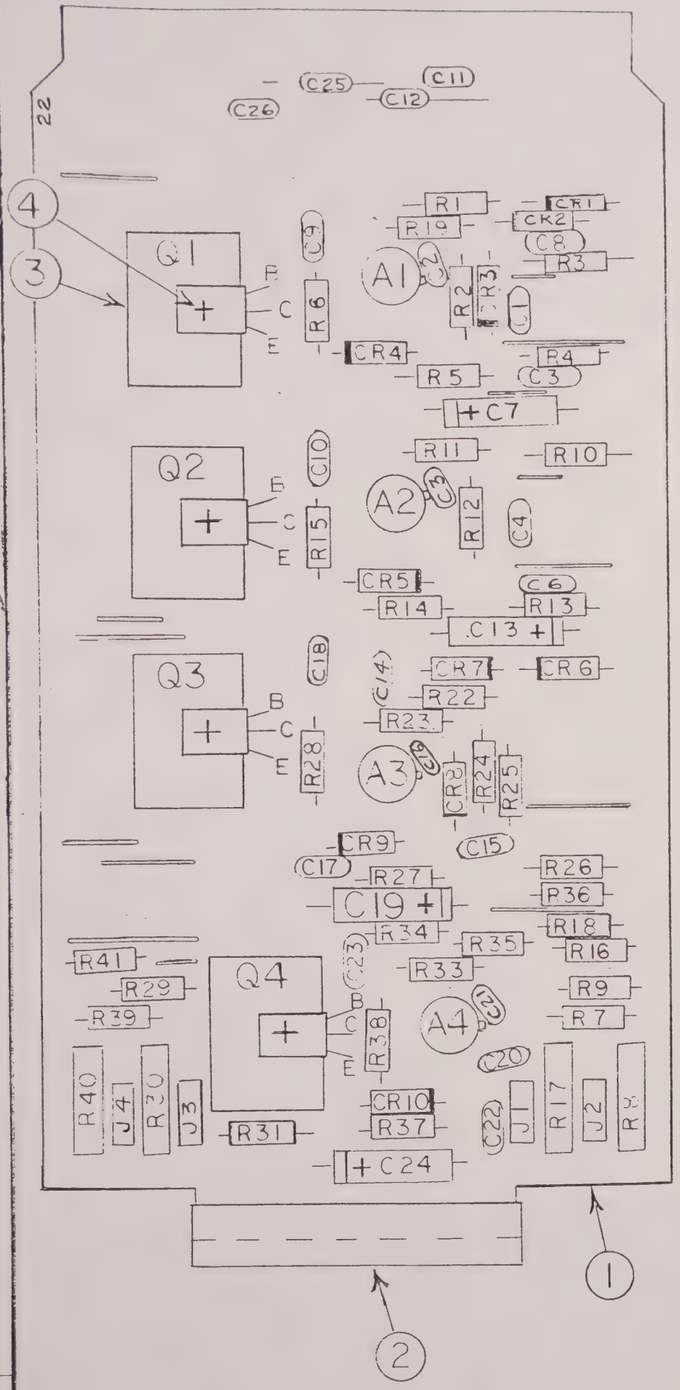
SCALE

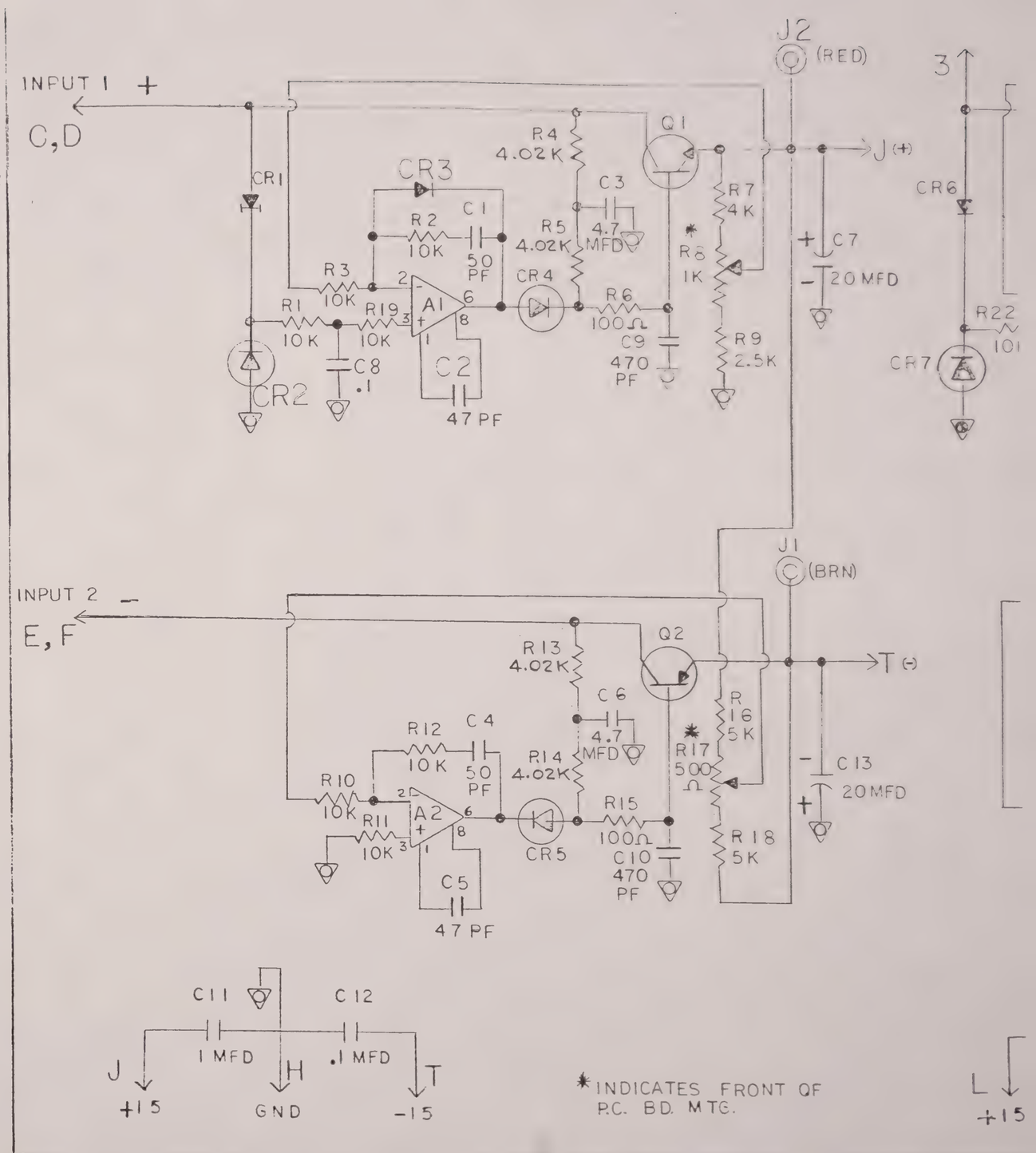
103376-5

IT	Q	PT NO	DESC	VEND
1	1	103377	P.C. BOARD	BAFCO
2	1	100078	HANDLE	"
3	4	PAI-ICB	HEATSINK	IERC
[illegible]		KF 2440	PRESS NUT	PEM
[illegible]	1	LM308	AMPLIFIER	NAT'L.
A3	1			
A4	1			
C11	1		1 MFD.	ERIE
C7	1			
C13	1	TT25X20	C: 20MF-25V	SPRAGUE
C19	1			
C24	1			
C25	1		1 MFD	ERIE
Q1	1	MJE-803		
Q2	1	MJE-703	TRANSISTOR H.V.	
Q3	1	MJE-803		
Q4	1	MJE-Y03		
CR2	1	IN825		
CR4	1	IN5236A		
CR5	1	IN5236A	DIODE, ZENER	MOTOROLA
CR7	1	IN825		
CR9	1	IN5236A		
CR10	1	IN5236A		
CR1	1	IN5314	DIODE	
[illegible]		IN5314	CONSTANT CURRENT	
[illegible]	1			
C26	1		.1 MFD	ERIE

NOTES:

1 - UNLESS OTHERWISE SPECIFIED,
ALL CAPS - ERIE
ALL RESISTORS - 1/4W, 1%
RN60D - CORNING.
ALL DIODES - FD666 - FAIRCHILD





*INDICATES FRONT OF P.C. BD. MTG.

NO	REVISIONS	
	R4,5,13,14,24,27,34,37 WAS 2K REV. DELETE U1, C27, C28	11-81
B	REDRAWN 8-26-81	S.S.
A	RELEASE 10-2-75	A.G.

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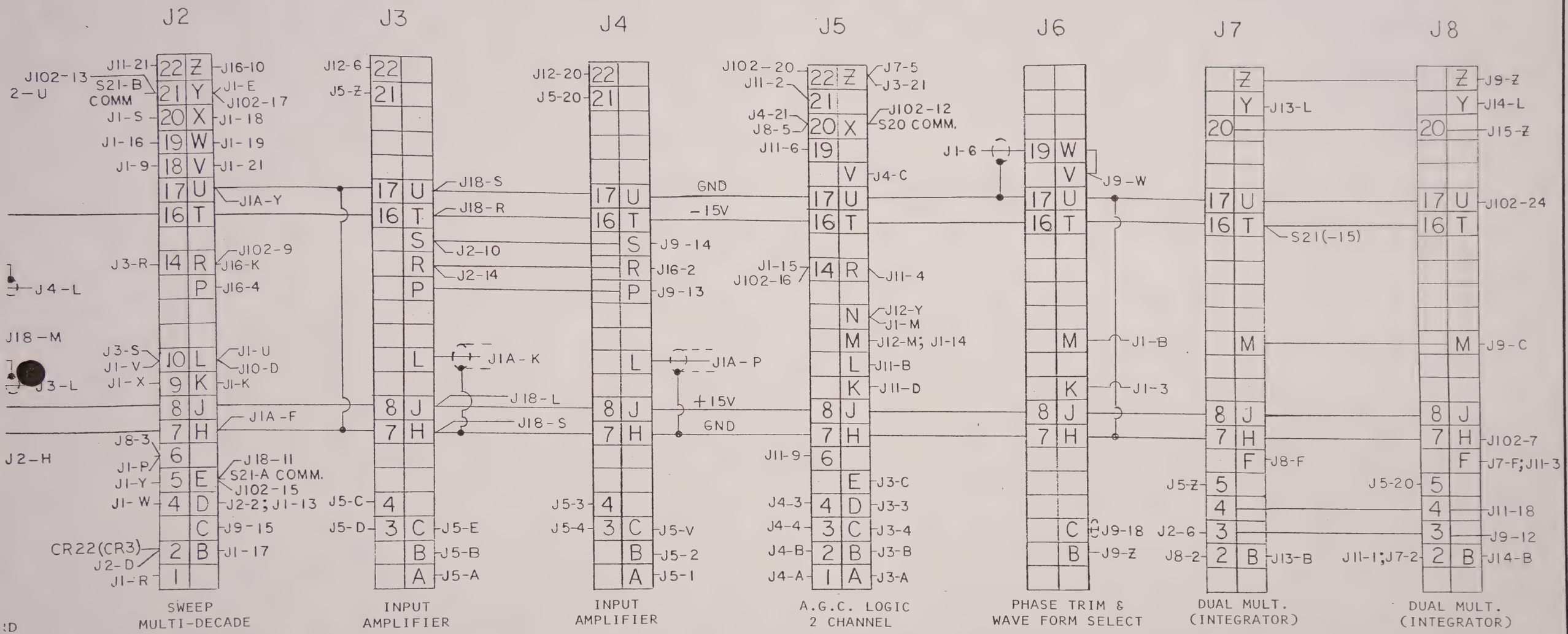
BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

A
SCHEM
MUL
MODEL 916H/S



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BAFCO, INC.

BAFCO, INC

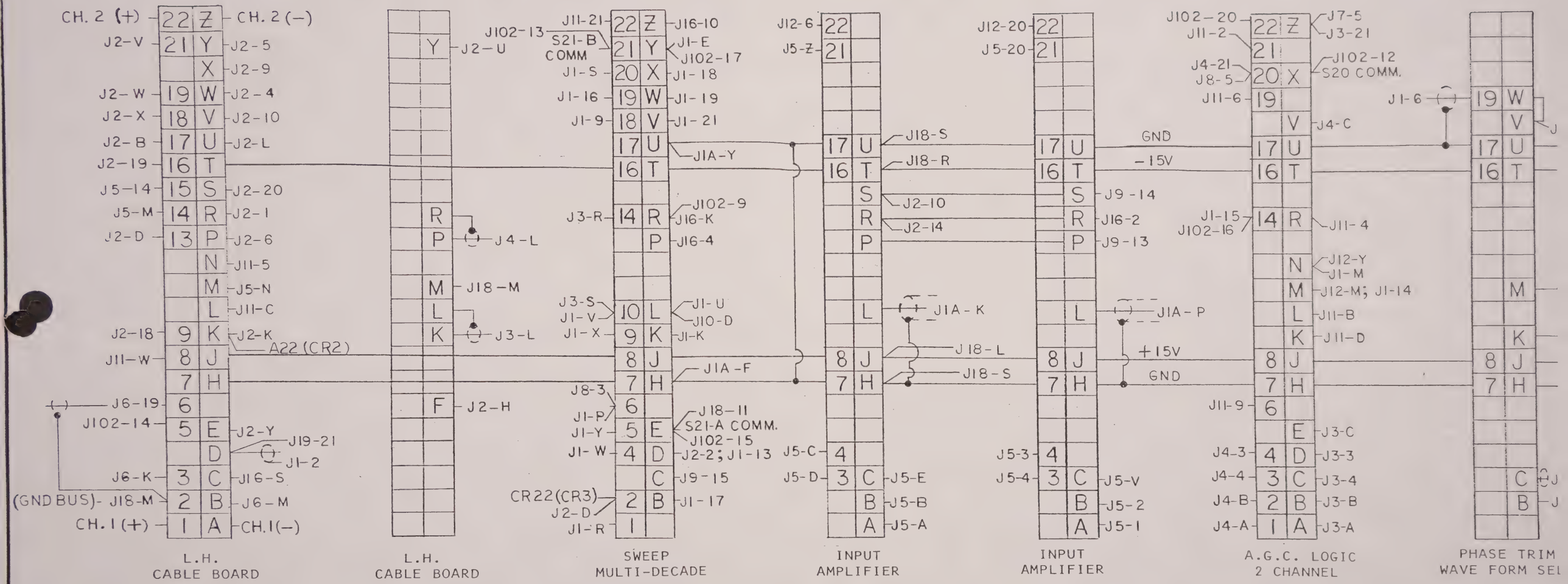
BY
DATE
APPD
DATE

ASSEMBLY
INTERCONNECTION DIAGRAM
MODEL 916XH REF

C
SCALE

103394-12
SH. 1 OF 4

IT	Q	PT NO	DESC	VEND



NO	REVISIONS	
B	REDRAWN 4-82	A.
A	RELEASE	

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BAFCO, INC.

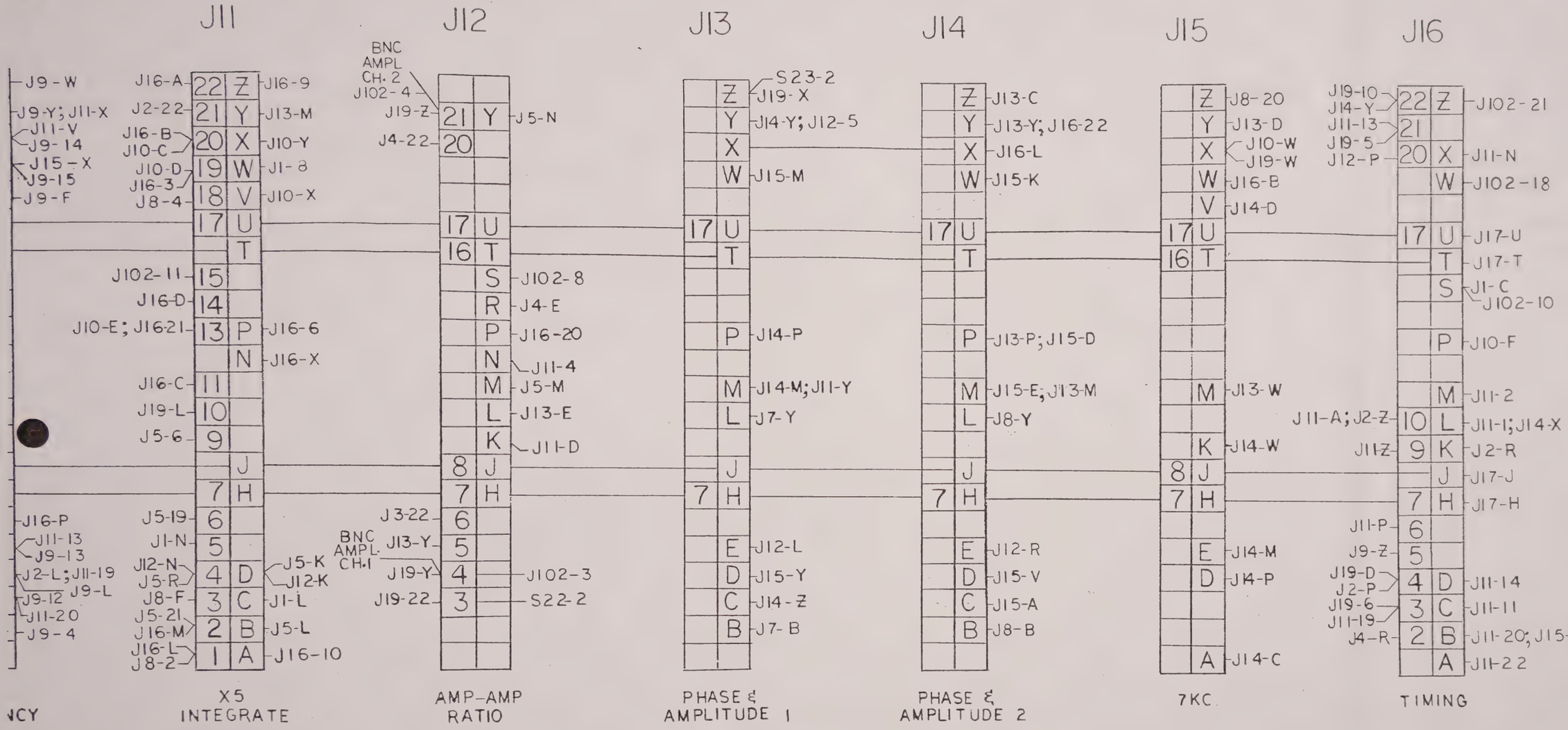
BAFCO, INC

BY	
DATE	
APPD	
DATE	

A

INTERC

MODEL 916



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BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

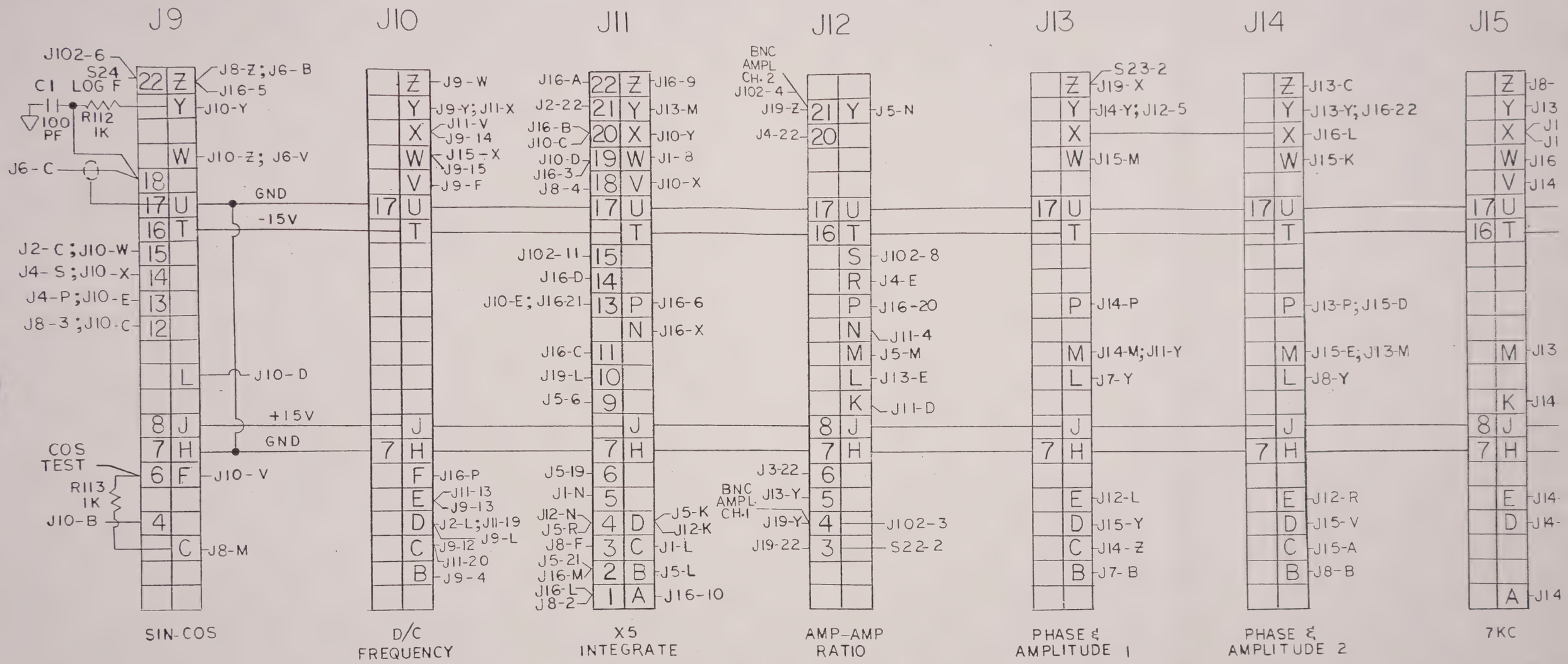
ASSEMBLY
INNERCONNECTION DIAGRAM
MODEL 916XH REF

C

SCALE
SH. 2 OF 4

103394-12

IT	Q	PT NO	DESC	VEND



NO	REVISIONS		
B	REDRAWN	4/13/82	L
A	RELEASE	12/1/75	

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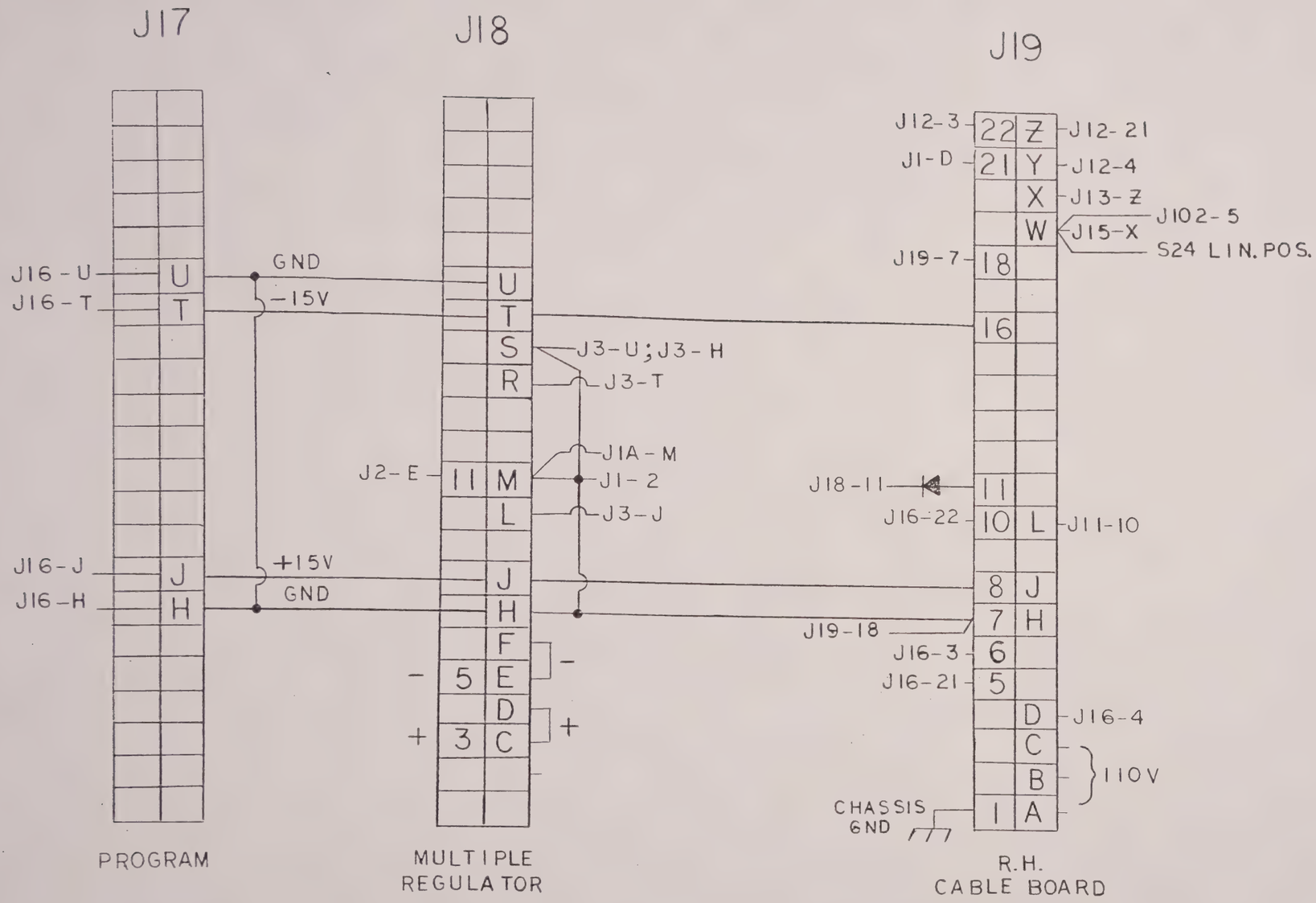
BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

A
INNERC(

MODEL 916X



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BAFCO, INC.

BAFCO, INC

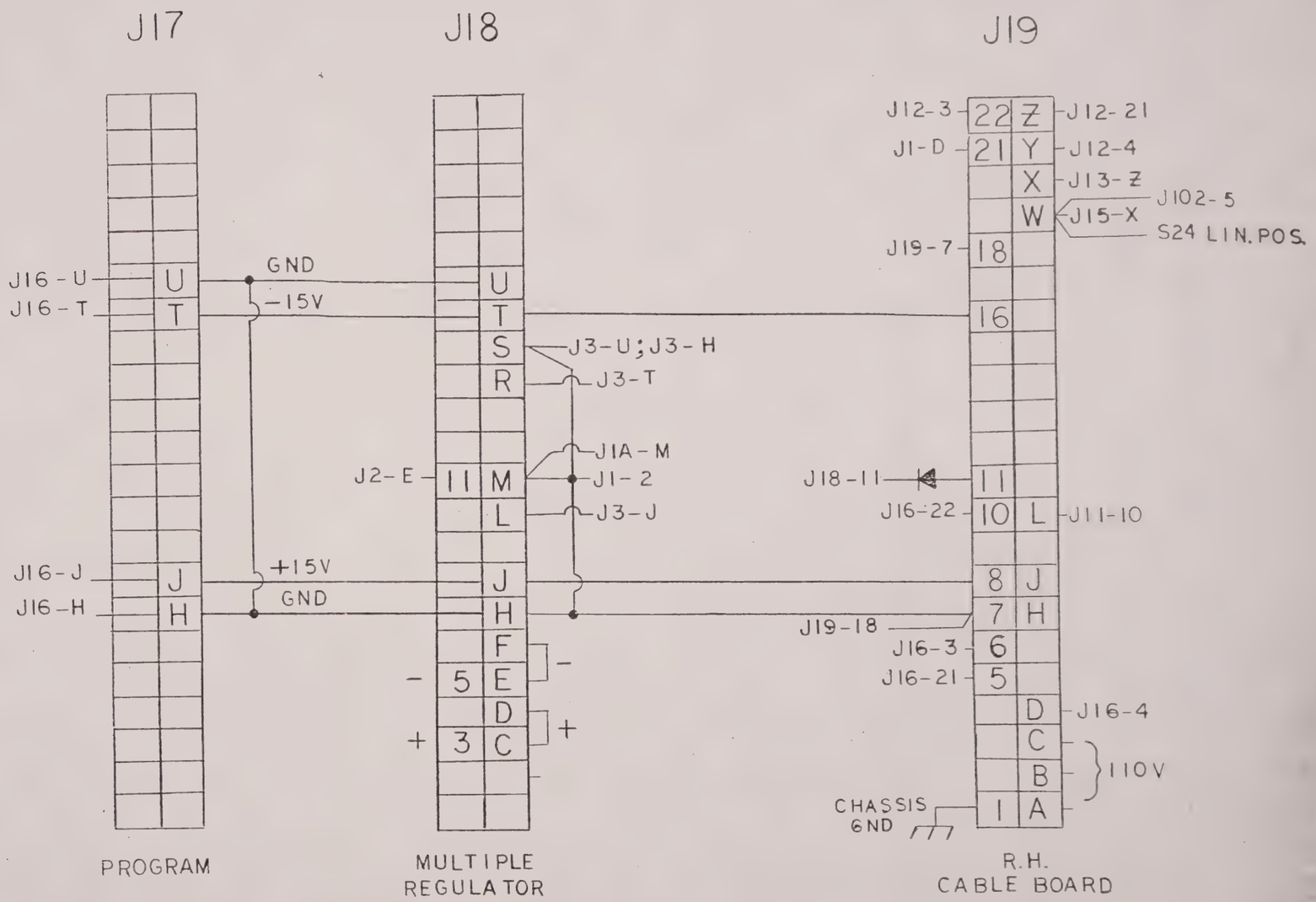
BY
DATE
APPD
DATE

ASSEMBLY
INNERCONNECTION DIAGRAM
MODEL 916XH REF

C
SCALE

103394-12
SH. 3 OF 4

IT	Q	PT NO	DESC	VEND



NO	REVISIONS	
B	REDRAWN	4-22-82 D.
A	RELEASE	12-1-75

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BAFCO, INC.

BAFCO, INC

BY
DATE
APPD
DATE

AI
INNERCO
MODEL 916XH

-J12-4

J10B

-J12-21

SWP IN
J2-E
CAL
J2-21
S21
-15

AGC IN
J5X
S20

J1B
J1-1
J2B
J1-A
J3B
J1-22
J4B
J1-Z

J5-B
OUTPUT
J1-D
J1-2

PLOTTER INTERFACE
A1

J102

REMOTE CONTROLS SEE SEC. 2.2 I.M.

J2-21	13	12	J5-X	REMOTE CONTROLS SEE SEC. 2.2 I.M.
J1-5	14	11	J11-15	
J2-E	15	10	J16-S	
J5-14	16	9	J2-R	END SWP.
J2-Y	17	8	J12-S	FLAG
J16-W	18	7	GND	GND
	19	6	J9-22	LOG F
J5-22	20	5	J19-W	LIN F
J16-Z	21	4	J9B (J12-21)	BNC db AMP. CH. 2
	22	3	J7B (J12-4)	BNC db AMP. CH. 1
-15 R108 500Ω	23	2	J6B	BNC A.R.
GND	24	1	J8B	BNC Δ∅

READOUT ANALOG

J11B
J9-6
COS

REMOTE READOUT & CONTROLS
A2

J105

8	7	
9	6	
10	5	K1-1 PIN 4 (N.O)
11	4	
12	3	K1-1 PIN 6 (N.C.)
13	2	
14	1	K1-1 PIN 3 (C)

14 PIN CONN. FOR
AUTO PEN-LIFT
REF. DWG. B104102

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BAFCO, INC.

BAFCO, INC

BY RASSI
DATE 12-1-75
APPD
DATE

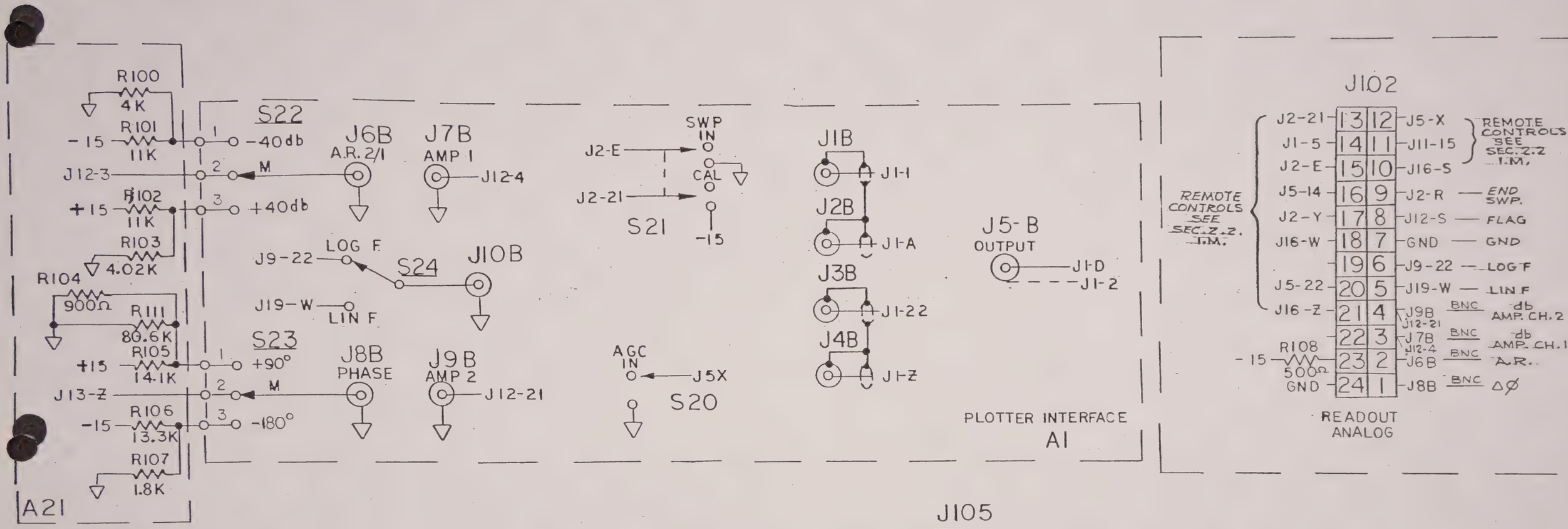
ASSEMBLY
INTERCONNECTION DIA.
MODEL 916 XH REF

C

SCALE —

103394-12
SH 4 OF 4

Q	PT NO	DEBC	VEND



J105

8	7
9	6
10	5 — K1-1 PIN 4 (N.O)
11	4
12	3 — K1-1 PIN 6 (N.C.)
13	2
14	1 — K1-1 PIN 3 (C)

14 PIN CONN. FOR
AUTO PEN-LIFT
REF. DWG. B104102

RELEASE 1-76 A.G.

REVISIONS

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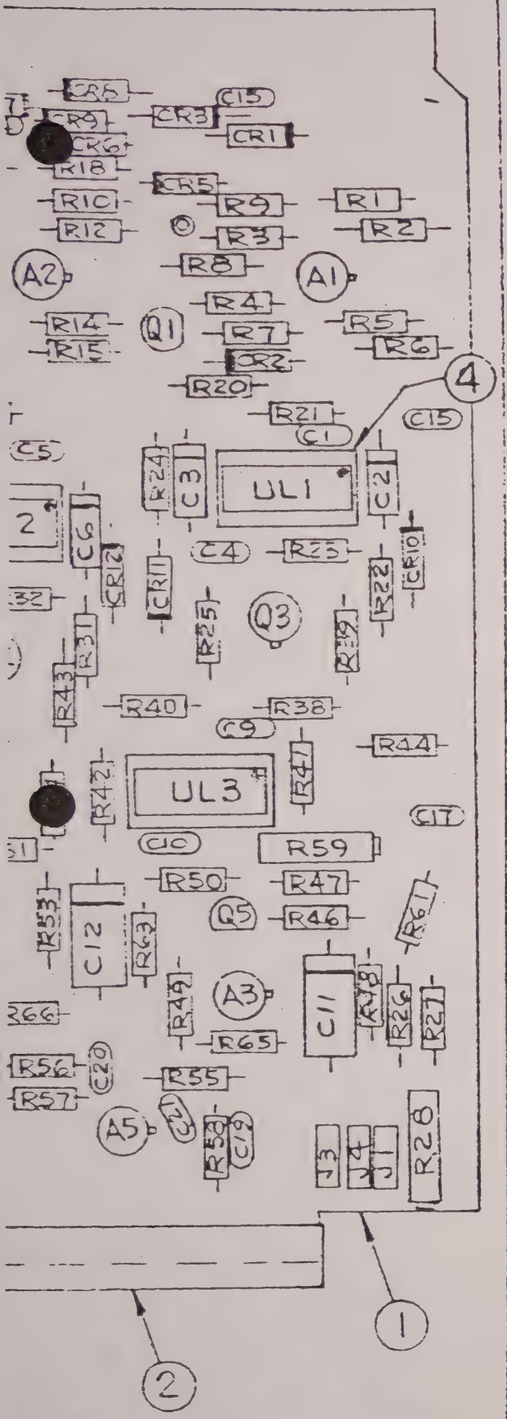
BAFCO, INC.

BAFCO, INC

BY RASSI
DATE 12-1-75
APPD
DATE

AS
INTERCO
MODEL 916 XF



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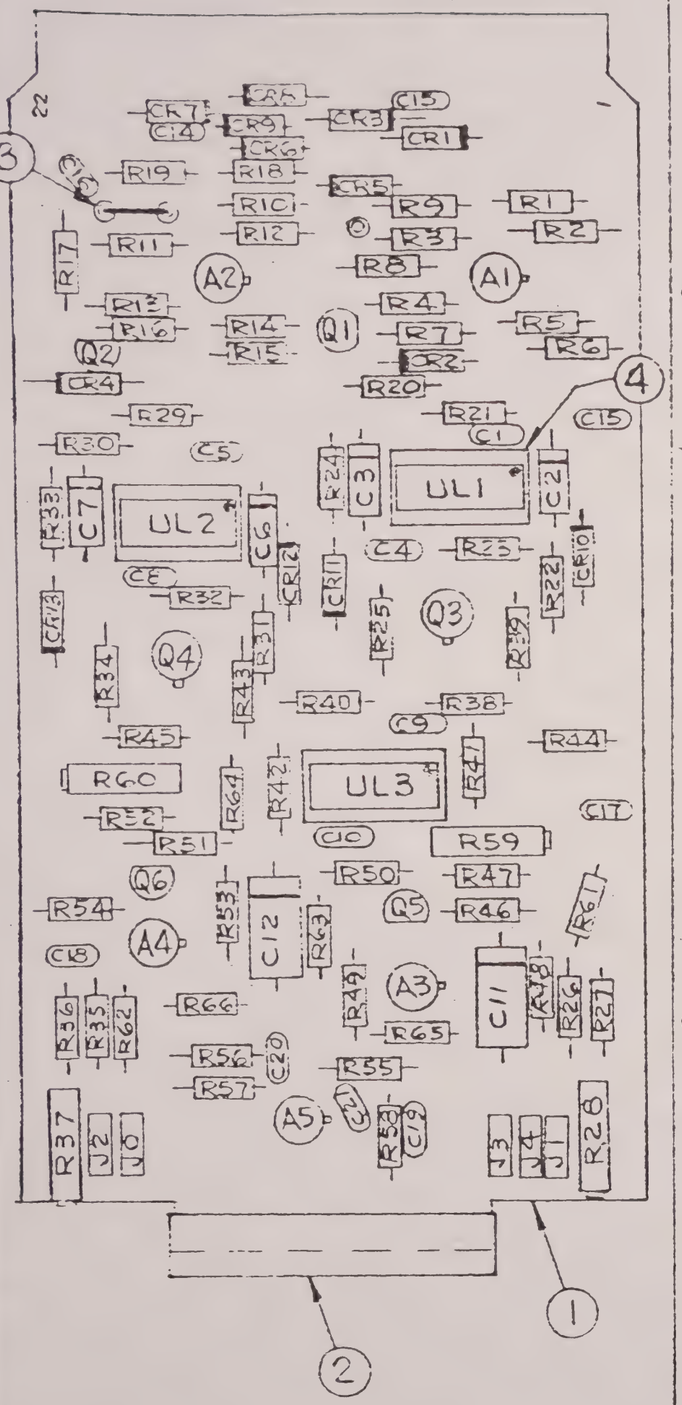
C	SCALE FULL
103395-5	

Q	PT NO	DESC	VEND
1	103396	P.C. BOARD	BAFCO
1	100073	HANDLE	"
		TERMINAL	CAMBION
	516-AG-11D	I.C. SOCKET	AUGAT
1	LH 2308	I.C. 16 PIN	NAT'L
1	"	I.C. 16 PIN	"
1	"	I.C. 16 PIN	"
1	LM1458	AMPLIFIER	NAT'L.
1	LM1458	↑	NAT'L.
1	3522J		BURR/BOW
1	3522J		" "
1	LM305	AMPLIFIER	NAT'L.
1	2N3905	TRANSISTOR	MOT
1	2N3905	"	MOT
1	726		
1	726		
1	TIS-75	TRANS-FET	MOT
1	TIS-75	TRANS.-FET	MOT
1	X463UW	.05 MF 10%	TRW
1	X463UW	.05 MF	↑
1	X463UW	.05 MF	
1	X463UW	.05 MF	
1	X663F	.47 MF	↓
1	X663F	.47 MF	TRW
1		10K .1%	I.R.C
1		↓	↓
1		10K .1%	IRC

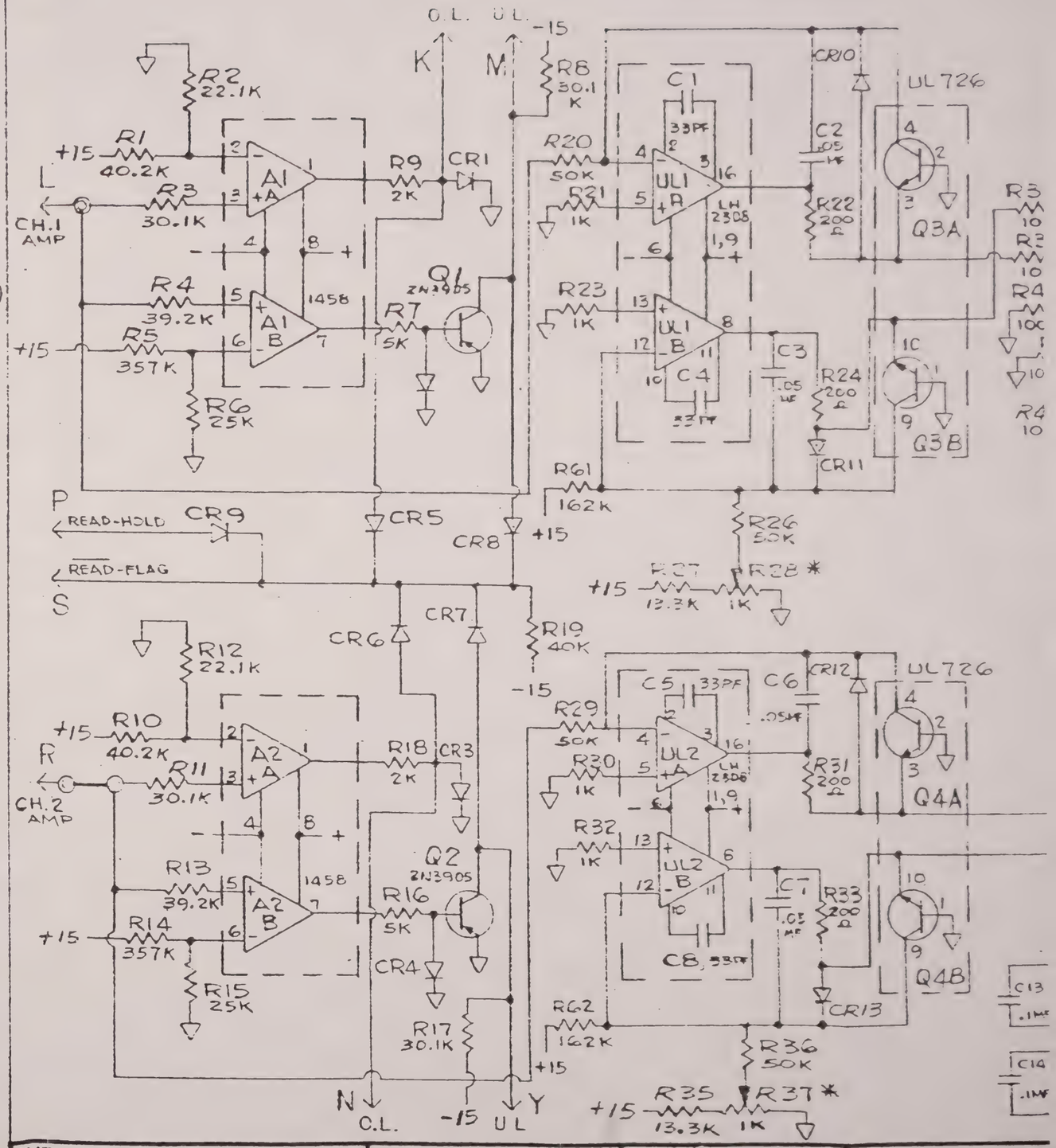
NOTES:
1 - UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS - ERIE.
ALL RESISTORS - 1/4 W 1%
RN60D - CORNING.
ALL DIODES - FD6666
FAIRCHILD.
ALL POTS - 89PR - BECKMEN
ALL JACKS - #430 [illegible]

REV.	4-76
REV. R65 & R66	2-76
REV.	2-76
RELEASE	

REVISIONS



* INDICATES FRONT P.C. MTG.



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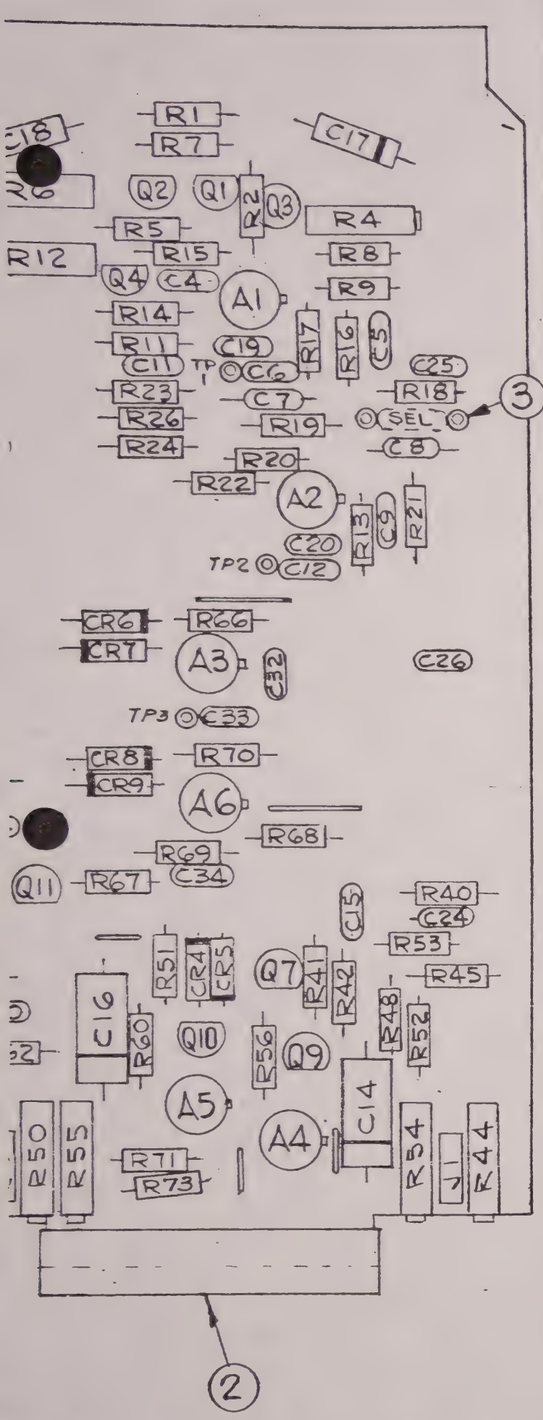
BAFCO, INC.

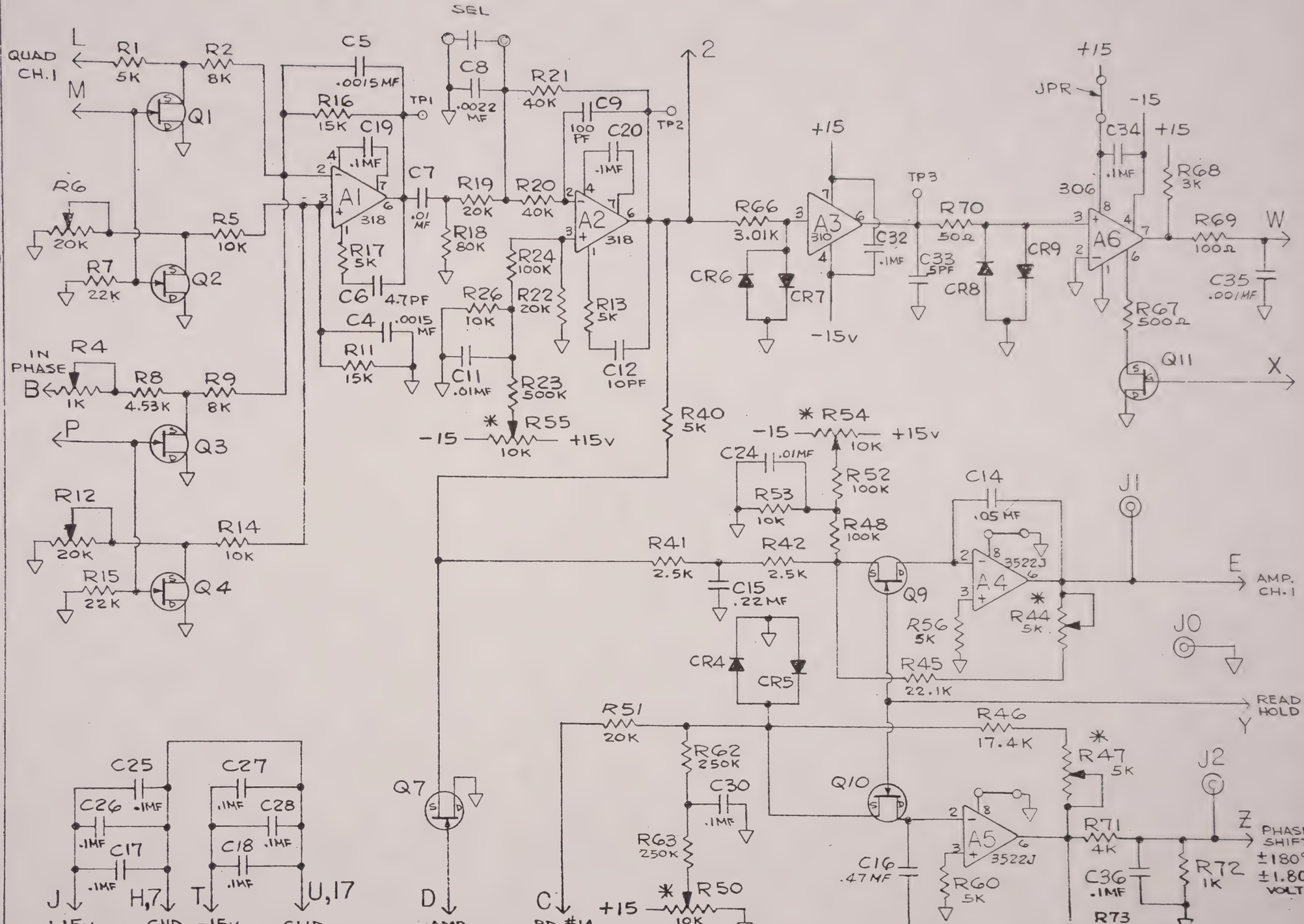
BAFCO, INC

BY [signature]
DATE 1-26-76
APPD
DATE

AS
SCHEMAT
AMP. & A
MODEL 916



ATES FRONT PANEL MTG.



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BAFCO, INC.

BAFCO, INC

BY GRASSI
DATE 1-24-76
APPD
DATE

ASSEMBLY #13
SCHEMATIC P.C. BOARD
PHASE & AMPLITUDE CH.1
MODEL 916 REF

C

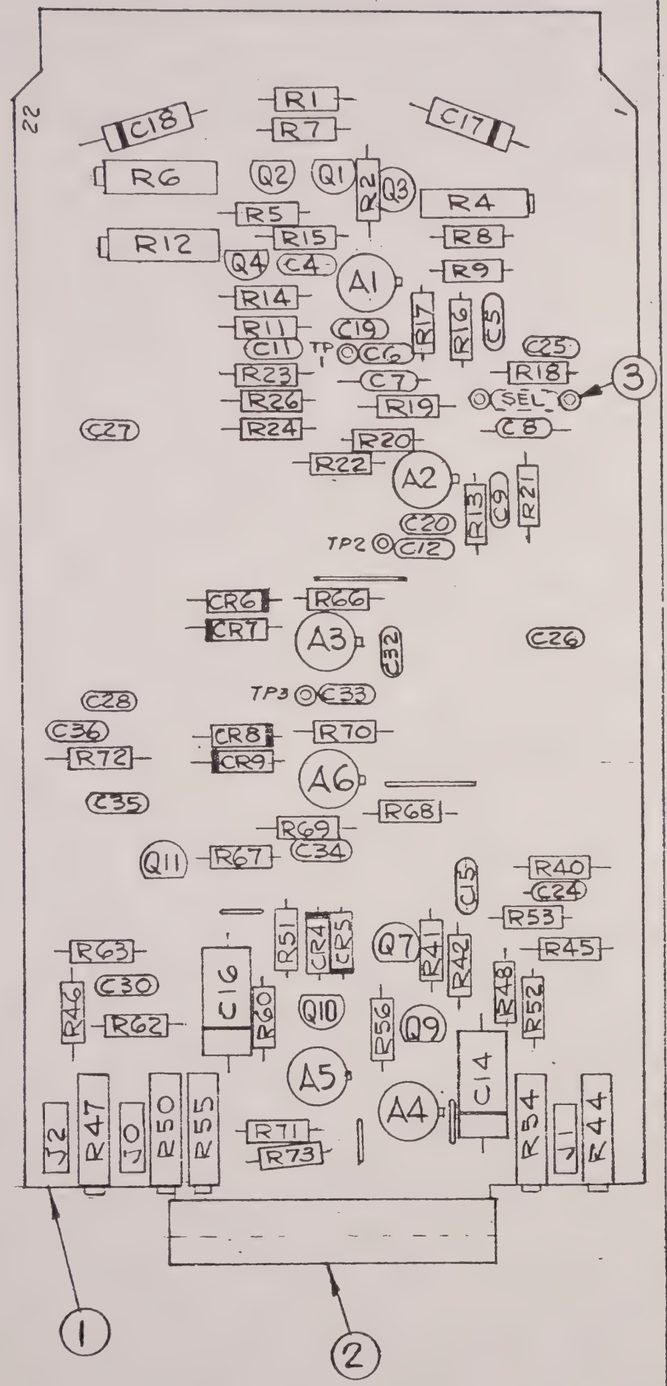
SCALE FULL

103401-1

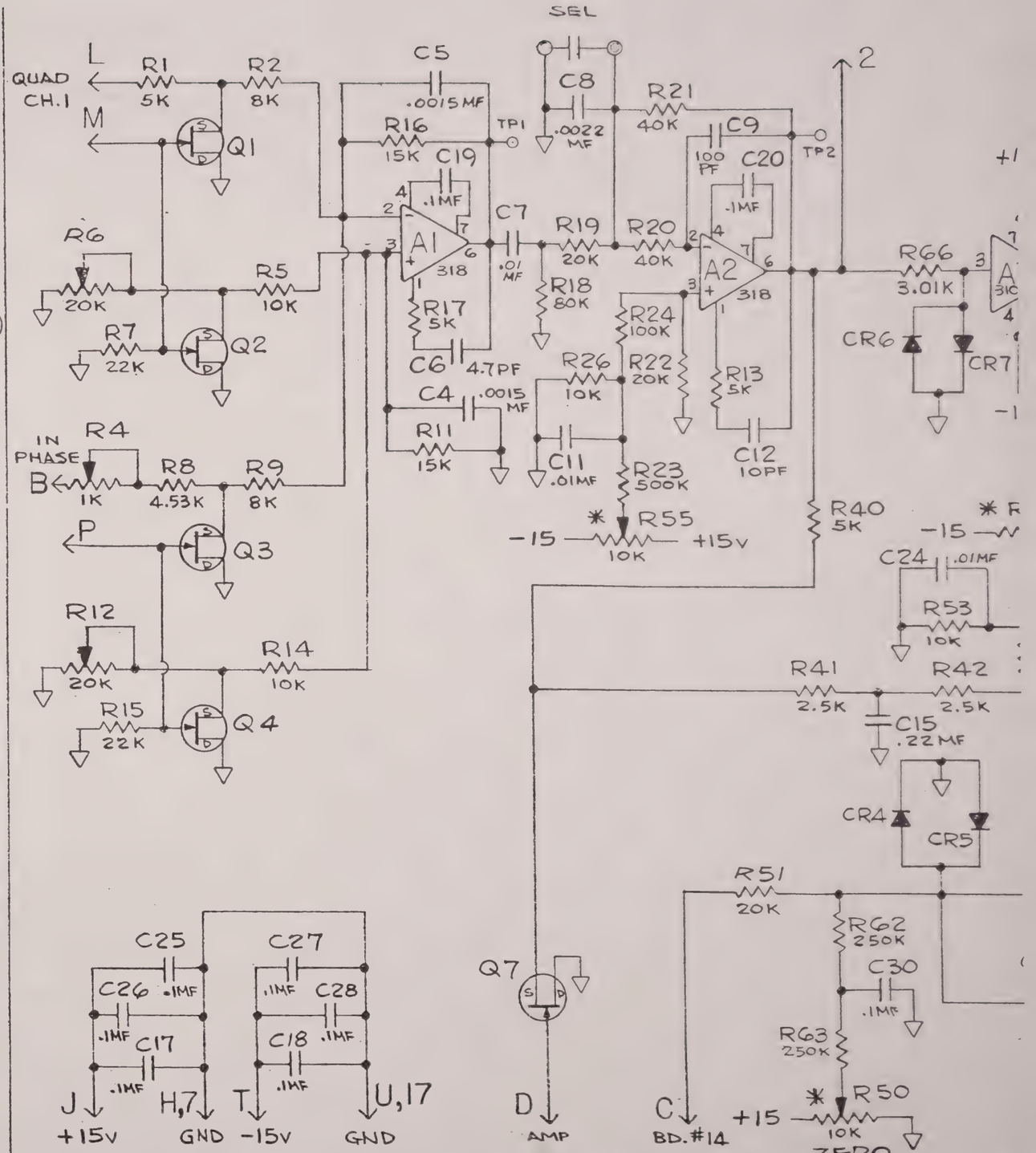
IT	Q	PT NO	DESC	VEND
1	1	103402	P.C. BOARD	BAFCO
2	1	100073	HANDLE	"
3	AR	160-1512-02 -05-00	TERMINAL	CAMBION
A1	1	LM318	AMPLIFIER	ADV. MIC
A2	1	LM318	"	" "
A3	1	LM310		NAT'L
A4	1	3522J		BURR/BRN
A5	1	3522J		" "
A6	1	LM306	AMPLIFIER	NAT'L
CR6	1			
CR7	1			
CR8	1	5082-2810	DIODE	SCHOTTKY HP
CR9	1			
C17	1			
C18	1	X663F	.1MF 100V 20%	TRW
C16	1		.47MF " 10%	"
C14	1	X463UW	.05MF " "	"

NOTES:

1-UNLESS OTHERWISE SPECIFIED:
- ALL CAPACITORS - ERIE
- ALL DIODES — FD6666 FAIRCHILD
- ALL RESISTORS - 1/4W, 1%
  - RN60D — CORNING
- ALL VAR. POTS 43P SPECTROL
- ALL TRANSISTOR FETS-U1899E
- ALL JACKS - #430 H.H.SMITH



* INDICATES FRONT PANEL MTG.



NO	REVISIONS
D	REV. RG4 DELETED 4-81
C	REV R73 ADD. 2/76
B	REV 2-76
A	RELEASE

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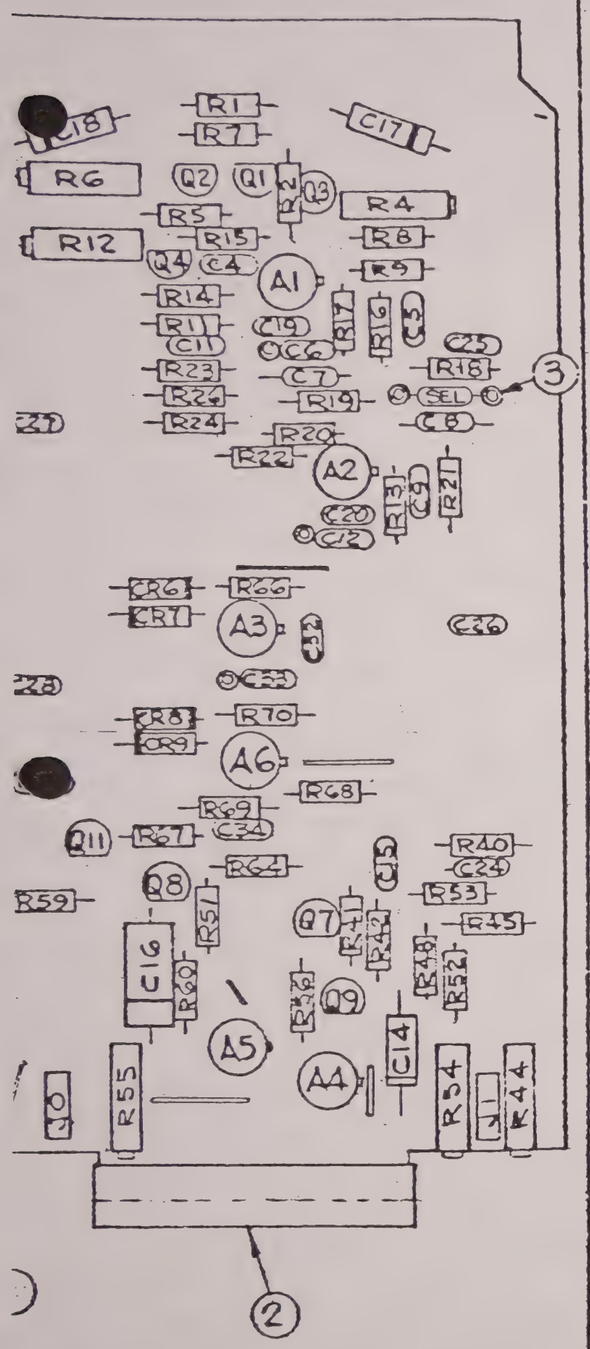
BAFCO, INC.

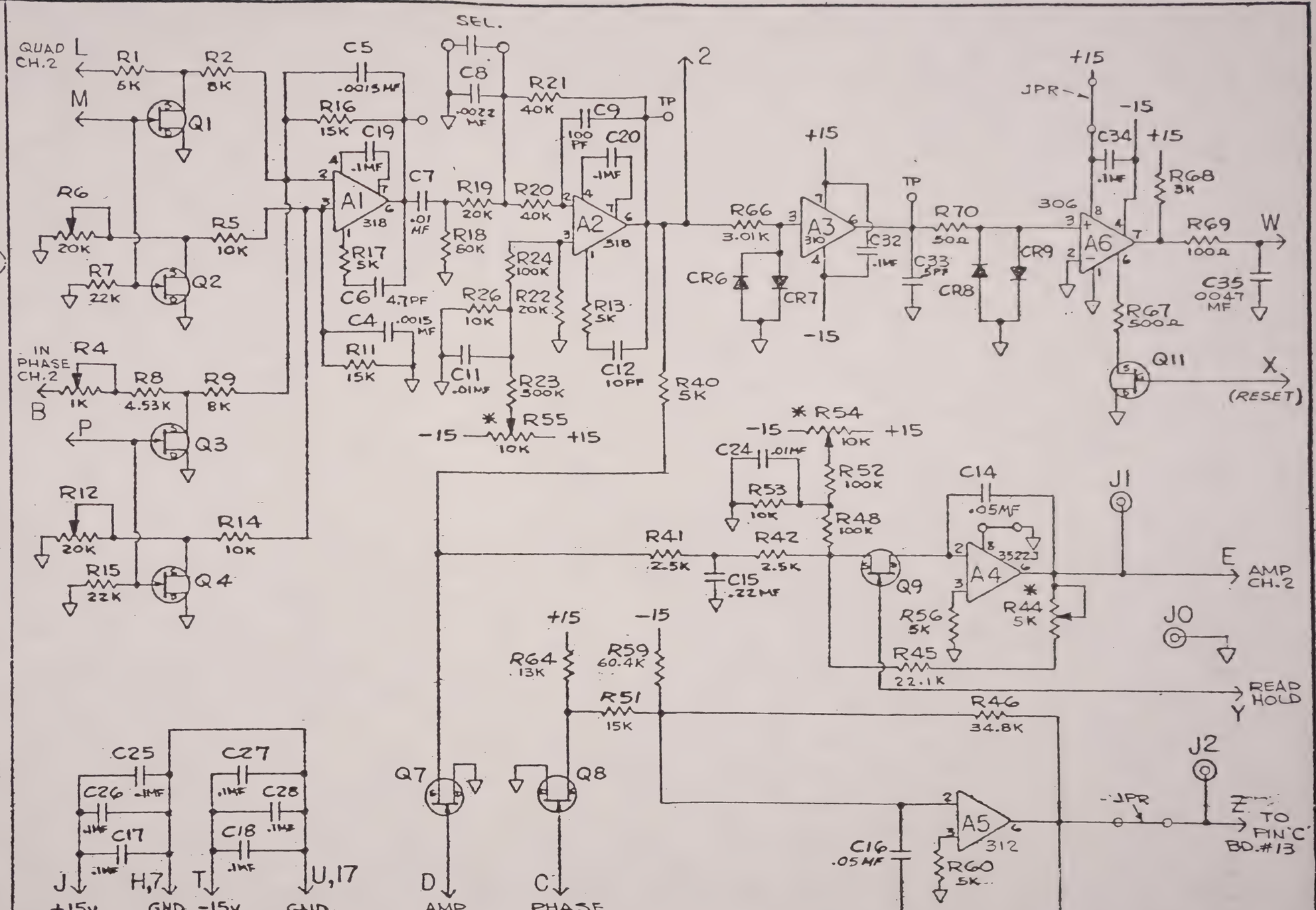
BAFCO, INC

BY GRASSI
DATE 1-24-76
APPD
DATE

SCHEMAT
PHA
MODEL 916



DICATES FRONT PANEL MTG.



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BAFCO, INC.

BAFCO, INC

BY BASSI
DATE 1-24-76
APPD
DATE

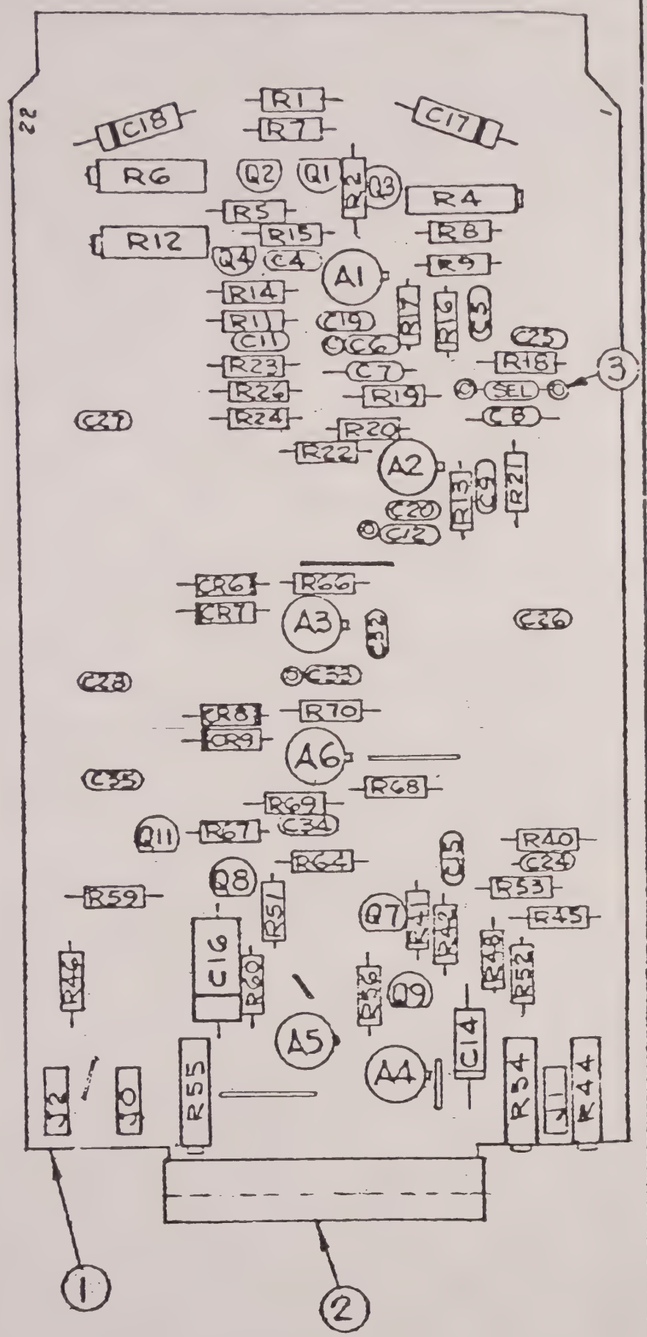
ASSEMBLY # 14
SCHEMATIC - P.C. BOARD
PHASE & AMPLITUDE CH.2
MODEL 916 REF

C
SCALE FULL
103401-2

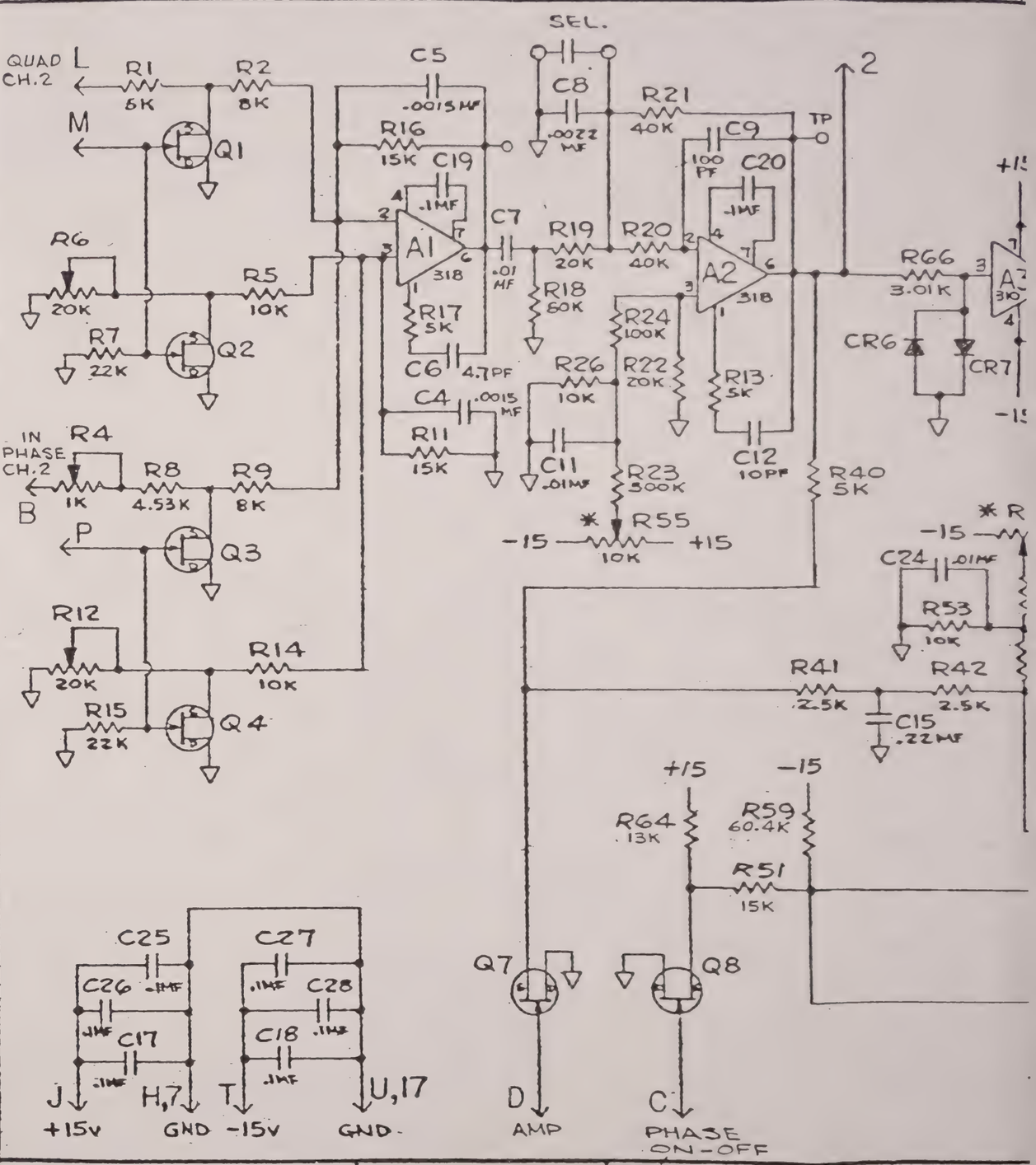
IT	Q	PT NO	DESC	VEND
1	1	103402	P.C. BOARD	BAFCO
2	1	100073	HANDLE	"
3	AR	160-1512-02-05-00	TERMINAL	CAMBION
A1	1	LM318	AMPLIFIER	ADV. MIC
A2	1	LM318	"	"
A3	1	LM310	↕	NAT'L
A4	1	3522J		BURR/BR
A5	1	LM312		NAT'L
A6	1	LM306	AMPLIFIER	NAT'L
CR6	1	5082-2810	DIODES	SCHOTTKY
CR7	1	"	"	"
CR8	1	"	"	"
CR9	1	"	"	"
C14	1	X463UW	.05 MF 100V 10%	TRW
C16	1			
C17	1	X663F	.1MF 100V 20%	"
C18	1			

NOTES:
1-UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS - ERIE
ALL DIODES - FDG666 FAIRCHILD
ALL RESISTORS - 1/4W, 1%
RN60D - CORNING.
ALL VAR. POTS - 89PR BECKMAN
ALL TRANSISTOR FETS TI-S75
ALL JACKS - #430 H.H. SMITH.

C	REV. 2-6-76	
B	REV 2-96	
A	RELEASE	
	REVISIONS	



* INDICATES FRONT PANEL MTG.



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BAFCO, INC.

BAFCO, INC

BY BASSI
DATE 1-24-76
APPD
DATE

A
SCHEMAT
PHAS
MODEL 916

REVISIONS NO	DESCRIPTION
A	RELEASE

ITEM	QTY	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOI
1	1	102925		PRINTED CIRCUIT BD.	BAFC
2	1	100073		HANDLE	"
3	AR		SS-4024-19B	CABLE — 24 GA.	SPECTR
4	2	516-AG-11D		I.C. SOCKET — 16 PIN	AUGUT
UL1	1		14585	I.C. 16 PIN (IN LINE)	MOT.
UL2	1		14585	I.C. 16 PIN " "	"
C50	1			C: .1 MFD	ERIE
C51	1			C: .1 MFD	"
C52	1			C: .1 MFD	"
C53	1			C: .1 MFD	"
CR1	1		FD6666	DIODE	FAIRCH
CR2	1		"	DIODE	"
R1	1		RN60D	R: 20K 1/4W. 1%	CORNIN
R2	1			R: 1.5K	
R3	1			R: 10K	
R4	1			R: 1K	
R5	1			R: 10K	
R6	1			R: 1K	
R7	1			R: 1K	
R8	1			R: 10K	
R9	1			R: 40.2K	
R10	1			R: 1K	
R11	1			R: 10K	
R12	1			R: 40.2K	
R13	1			R: 1K	
R14	1		RN60D	R: 1K 1/4W. 1%	CORNIN

PARTS LIST

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BAFCO, INC.

BAFCO, INC

ASSEMBLY
P.C. L.H. CABLE BOARD

MODEL 916

BY GRASSI
DATE 2-10-76

APPD
DATE

A

SH 1 OF 2

103412

REVISIONS NO	DESCRIPTION
A	RELEASE

ITEM	QTY	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOR
R15	1		RN60D	R: 20K 1/4W 1%	CORNING
R16	1		↕	R: 20K ↕	↕
R17	1		↕	R: 20K ↕	↕
R18	1		↕	R: 1.5K ↕	↕
R19	-		↕	↕	↕
R20	-		↕	↕	↕
R21	-		↕	↕	↕
R22	1		↕	R: 20K ↕	↕
R23	1		↕	R: 20K ↕	↕
R24	1		RN60D	R: 20K 1/4W 1%	CORNING
Q1	1		2N3905	TRANSISTOR – PNP	MOT.
Q2	1		"	"	"
Q3	1		"	"	"
Q4	1		"	"	"

PARTS LIST

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BAFCO, INC.

BAFCO, INC.

ASSEMBLY
P. C. L.H. CABLE BOARD

MODEL 916

BY STRASSI
DATE 2-10-76

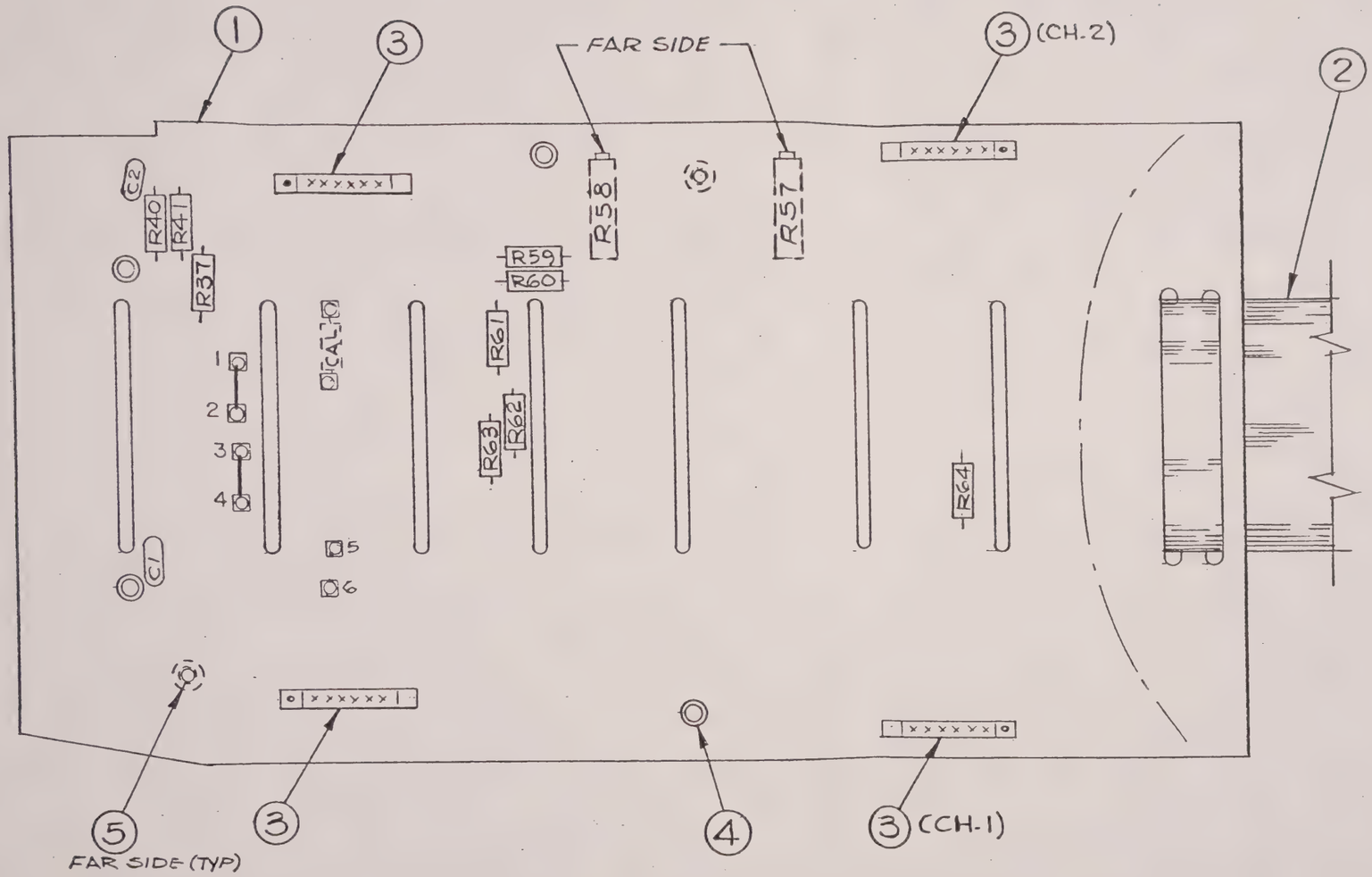
APPD
DATE

A

SH. 2 OF 2

103412

NO	DESCRIPTION	BY	DA
A	RELEASE		
B	REV.		2-74
C	REV		5-7



—— STANDARD
--- CARRIER (OPTION)

UNLESS OTHERWISE SPECIFIED FRACTIONS ± .015 TWO PL. DEC. ± .010 THREE PL. DEC. ± .005 ANGLES ±1/2 DEG. SUR. FIN. 125 MICROINCH	THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	**BAFCO, INC**	ASSEMBLY- P.C. SWITCH MOTHER BOARD MODEL 916H	BY GRASSI DATE 9-26-74 APPD DATE	B SCALE FULL 103414-5

REVISIONS NO	DESCRIPTION
A	RELEASE

ITEM	QTY	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOR
1	1	103029		P.C. BOARD	BAFCO
2	AR		#SS-4024-19B	CABLE - 24GA.	SPECTRA
3	4		00-8129-015-612-002	P.C. CONN.	ELCO
4	4		MR43	EYELET - MR43	MARK
5	2		KF2440	PEM NUT #4-40	PEM
C1	1		8121-100	C: .01MFD	ERIE
C2	1		8121-050-651-104	C: .1MFD	"
R37	1		RN60D	R: 45K	CORNING
R40	1		RN60D	R: 500Ω	CORNING
R41	1		RN60D	R: 500Ω	CORNING
R57	1		89PR	R: VARIABLE 2K	BECKMAN
R58	1		89PR	R: " 2K	"
R59	1		RN60D	R: 2K 1/4W 1%	CORNING
R60	1		↑	R: 500Ω	↑
R61	1			R: 833Ω	
R62	1			R: 1670Ω	
R63	1			R: 5K	
R64	1		RN60D	R: 1K	CORNING

PARTS LIST

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BAFCO, INC.

BAFCO, INC.

ASSEMBLY
P.C. SWITCH MOTHER BOARD

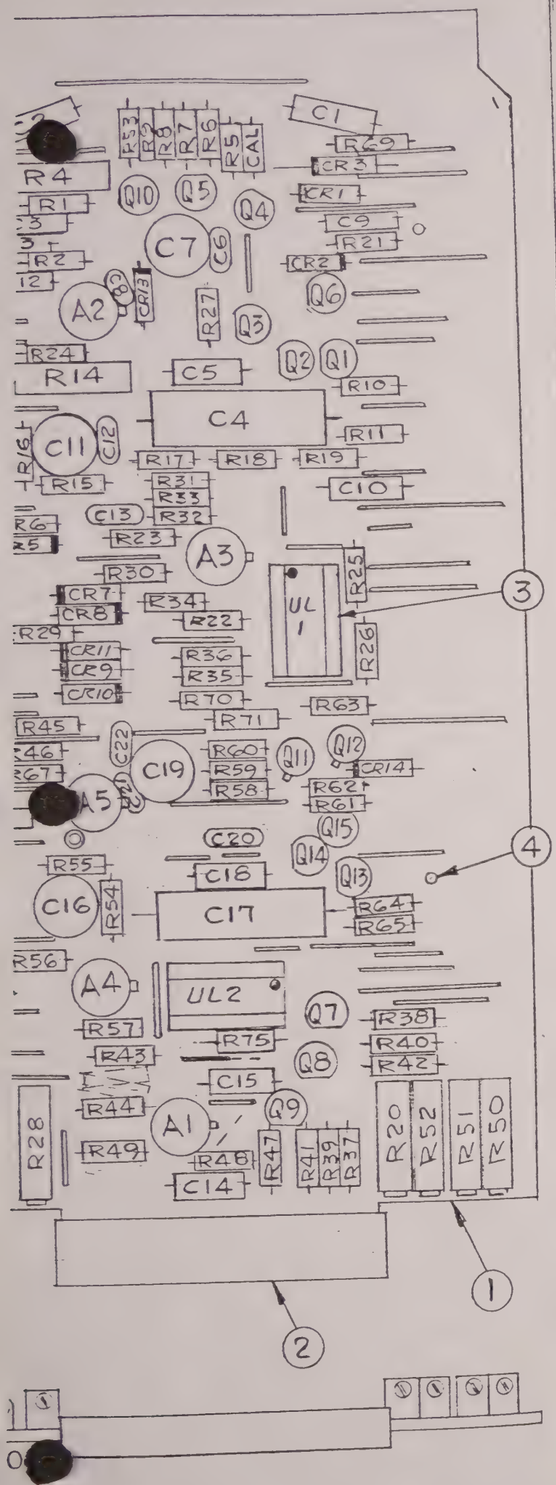
MODEL 916

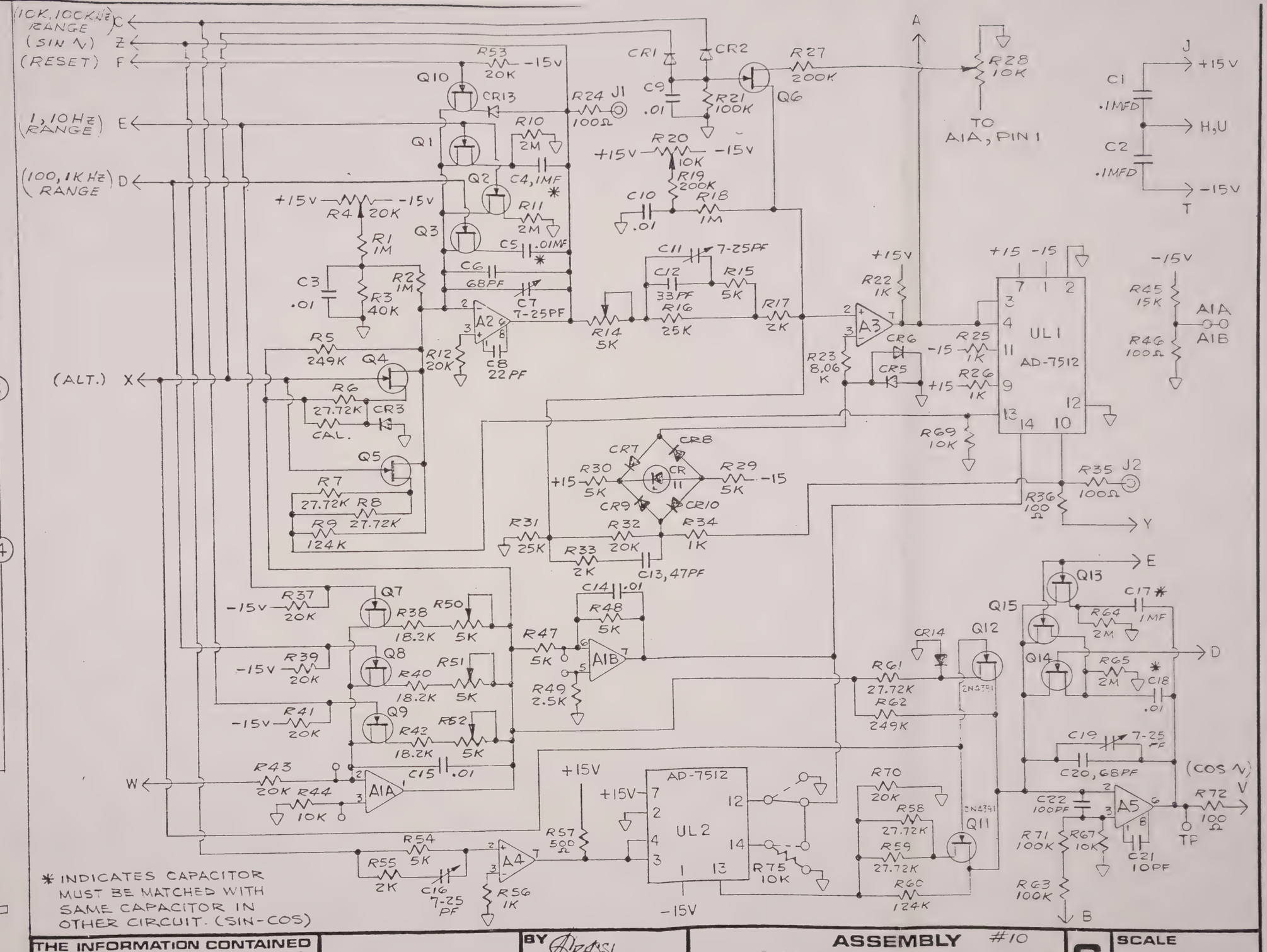
BY GRASSI
DATE 2-10-76

APPD
DATE

A

103415





* INDICATES CAPACITOR MUST BE MATCHED WITH SAME CAPACITOR IN OTHER CIRCUIT. (SIN-COS)

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BAFCO, INC.

BAFCO, INC

BY Brassi
DATE 20 MAR. '81
APPD
DATE

ASSEMBLY #10
SCHEMATIC - P.C. BOARD
DC/FREQUENCY (100KC)
MODEL 916XH **REF**

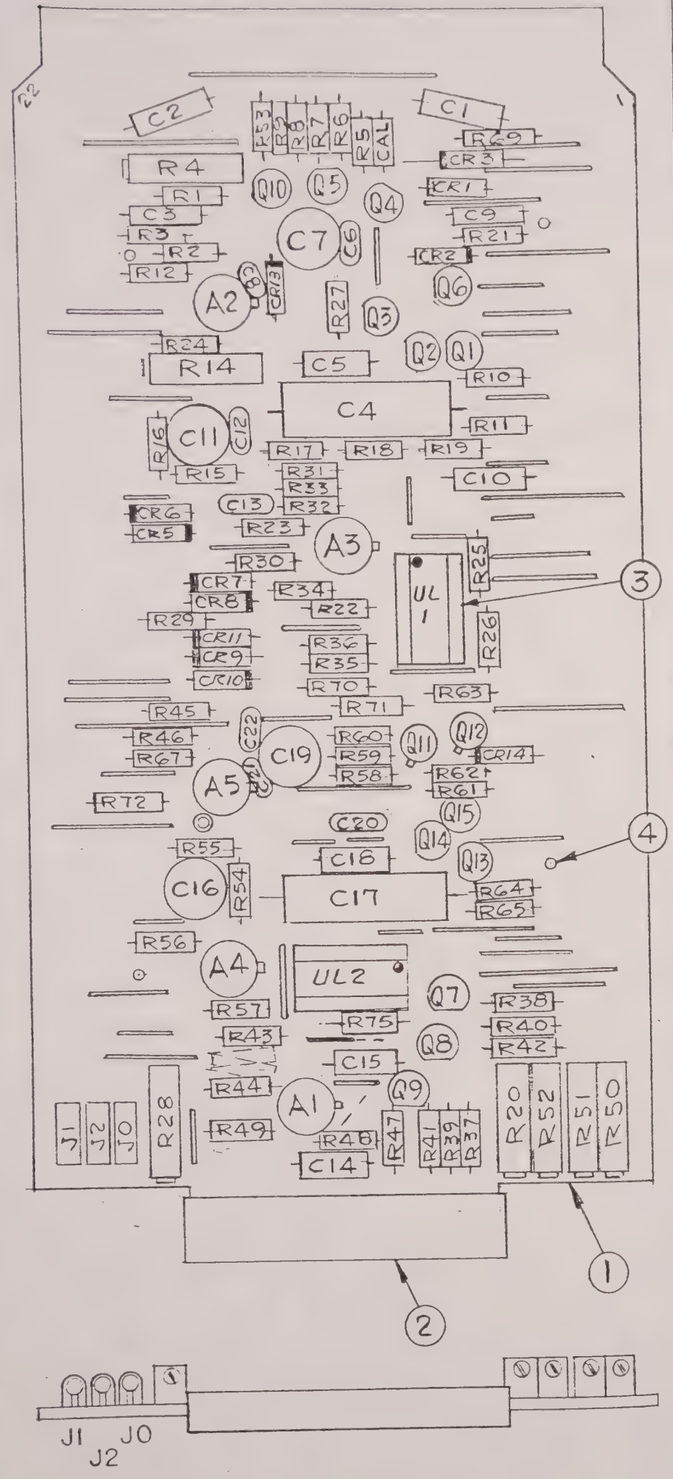
C

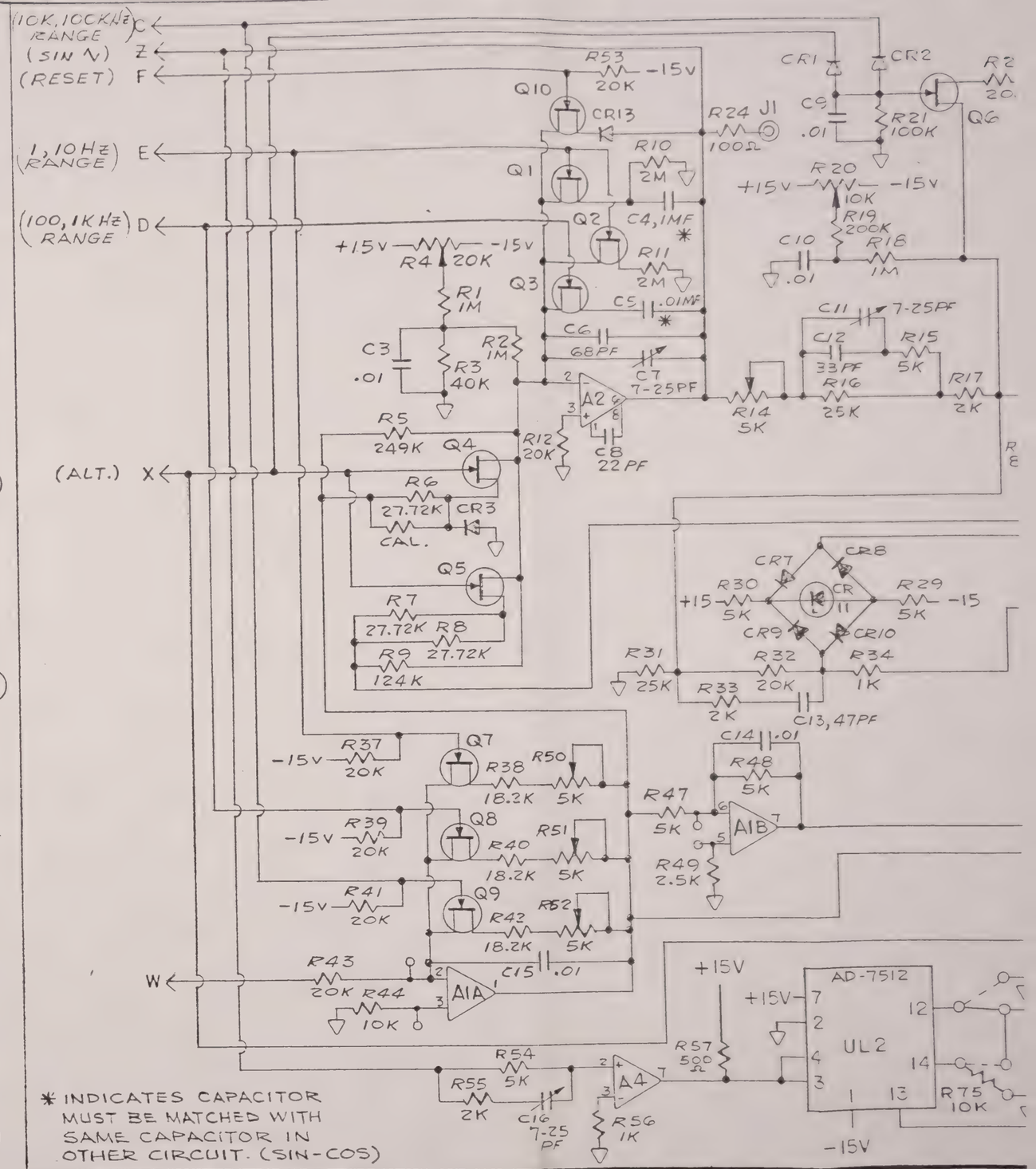
SCALE FULL

104470

IT	Q	PT NO	DESC	VEND
1	1	104471	PC. BOARD	BAFCO
2	1	100073	HANDLE	"
3	1	514-AG11D	I.C. SOCKET	AUGAT
[illegible]	1	AD642	DUAL AMP.	ANAL. DEV.
A2	1	CA3100T	AMPLIFIER	RCA
A5	1			
A3	1	LM 306	AMPLIFIER	NAT'L.
A4	1	LM 306		
4	4	120-1372	PIN	CAMBION
C1	1		C: .1MFD ±10%	S&EI
C2	1		C: .1MFD ±10%	
C3	1			
C5	1			
C9	1			
C10	1		.01MFD ±10%	S&EI
C14	1			
C15	1			
C18	1			
C4	1		C: 1MFD ±10%	S&EI
C17	1		C: 1MFD ±10%	
C7	1			
C11	1		7-25 PF	ERIE
[illegible]	1			
[illegible]	1			
CR4	1	IN5314	DIODE, ZENER	MOT.
CR11	1	IN825	DIODE, ZENER	MOT.
UL1	1	AD-7512	I.C. 14 PIN	ANALOG
UL2	1			
Q11	1	2N4391	TRANS-FET	MOT.
Q12	1			

NOTES:
1- UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS - RN55, 1/4W, 1%
ALL CAPS - ERIE
ALL DIODES - FD6666 - F'CHILD.
ALL VAR. POTS 43P - SPECTROL
ALL TRANSISTORS - FET U1899E
SILICONEX





* INDICATES CAPACITOR MUST BE MATCHED WITH SAME CAPACITOR IN OTHER CIRCUIT. (SIN-COS)

NO	REVISIONS
D	REV. C12 WAS 22 PF 5-82
C	REV. C8 WAS 10PF 2-82
B	REV. R75 ADD. 12/81
A	REV. 5-81
	RELEASE

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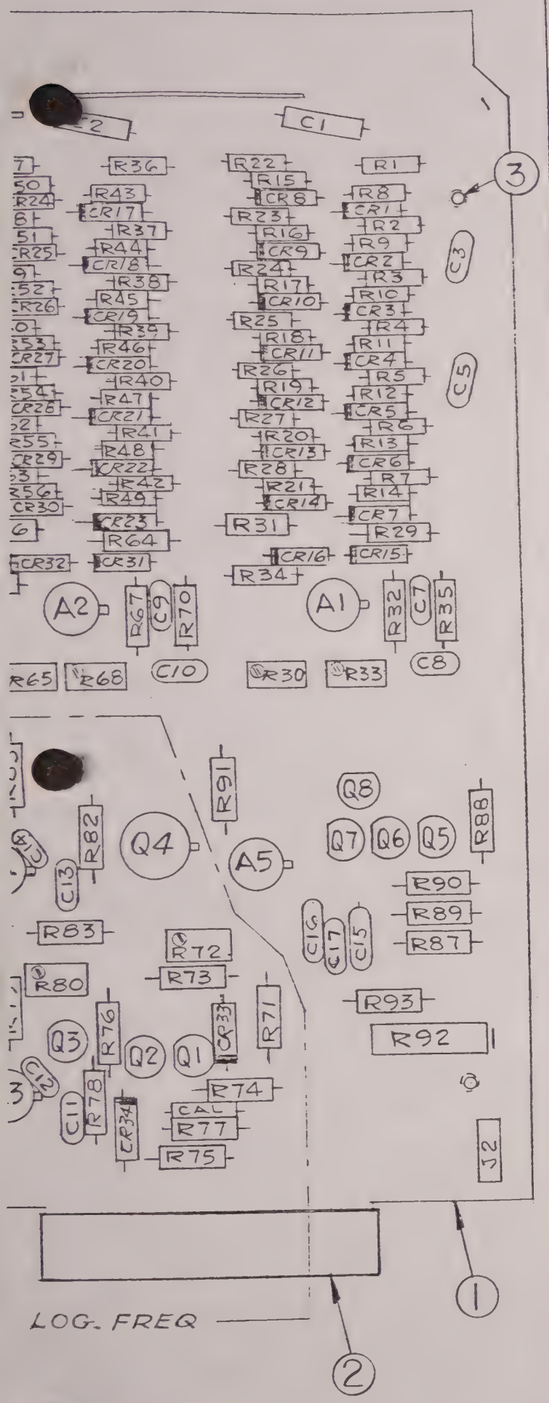
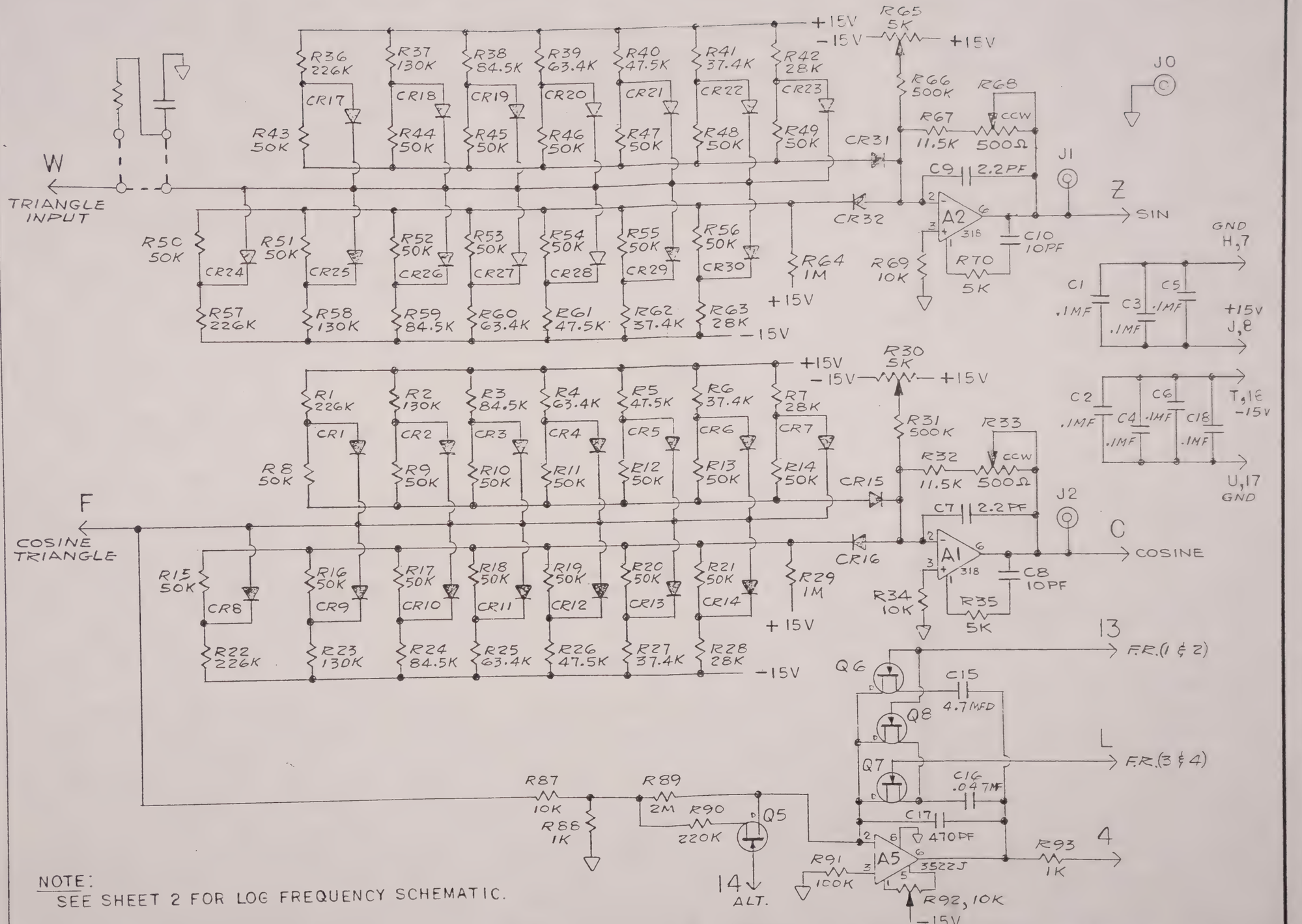
BAFCO, INC.

BAFCO, INC

BY [illegible]
DATE 20 MAR. '81
APPD
DATE

SCHE
DC/ FRE
MODEL 916





NOTE:
SEE SHEET 2 FOR LOG FREQUENCY SCHEMATIC.

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BAFCO, INC.

BAFCO, INC

BY BEASSI
DATE 25 MAR. '81
APPD
DATE

ASSEMBLY #9
SCHEMATIC - P.C. BOARD
COSINE GENERATOR - SIN/COS
MODEL 916XH **REF**

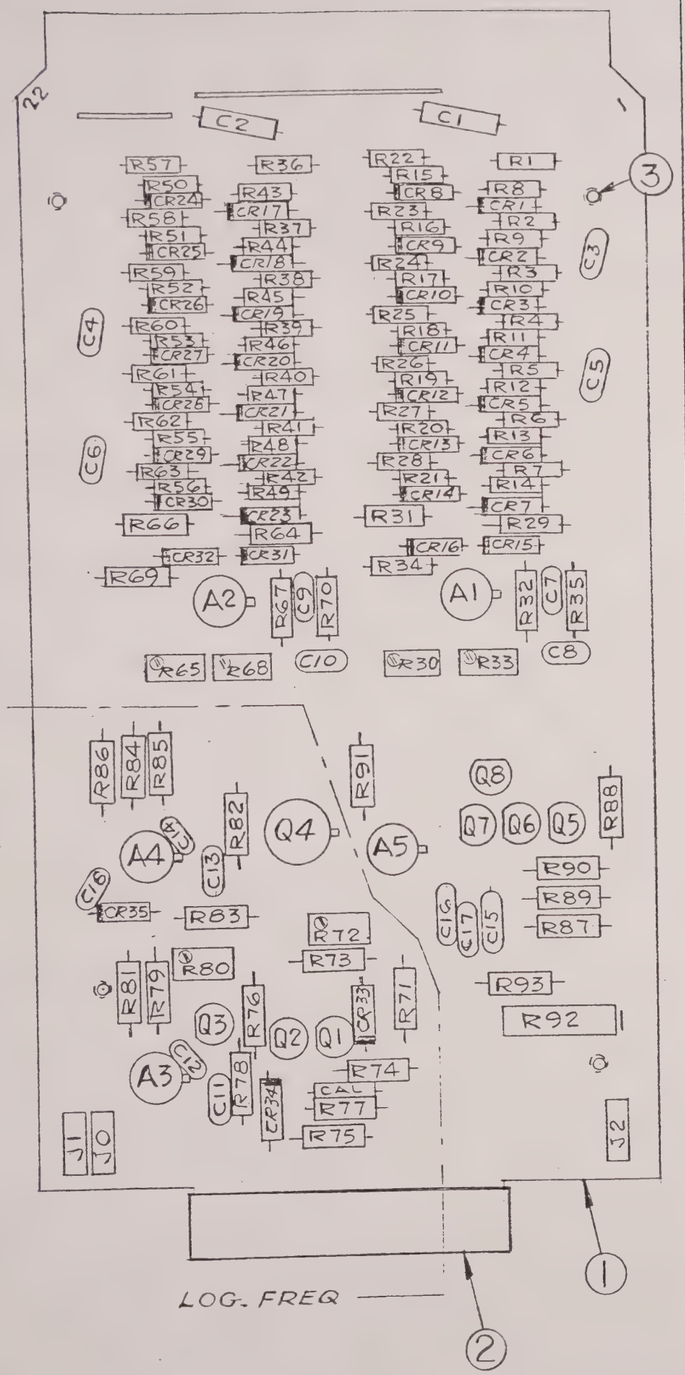
C | SCALE FULL

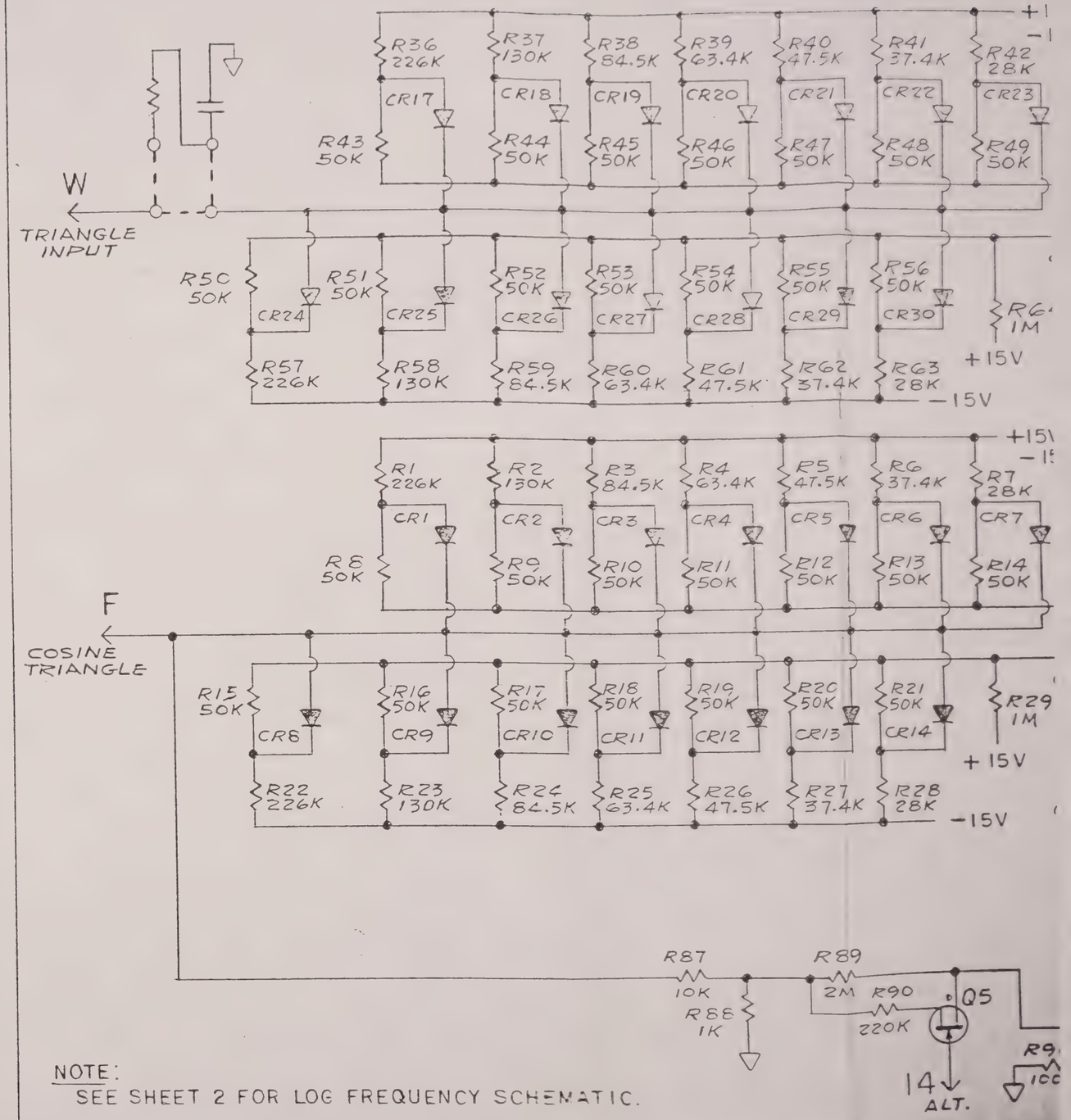
104473
SH. 1 OF 2

Q	PT NO	DESC	VEND
1	104474	P.C. BOARD	BAFCO
1	100073	HANDLE	"
1	LM318	} AMPLIFIER	NAT'L
2	LM318		NAT'L.
3	LM308		NAT'L.
4	LM308		NAT'L.
5	3522J		BURR/BRN
3	120-1372-02 03-000	TERM.	CAMBION
1		C: .1MFD } S&EI	
2		C: .1MFD	
4	UA726	TRANS. DUAL	NAT'L.
30		R: 5K VAR POT } BECKMAN	
33		R: 500Ω " "	
65	#66WR	R: 5K " "	
68		R: 500Ω " "	
72		R: 2K " "	
80		R: 1K " "	
74		R: 500K 1/4W 1% } I.R.C.	
75		R: 500K "	
76		R: 1M "	
78		R: 133K "	
R1 THRU R29 R36 THRU R63		} RN55D 1/4W, 10% CORNING	
23			
24			
25	U1899E	} TRANSISTOR	SILICONIX
26			
27			
28			

NOTE:
1-UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS 1/4W, 1%
RNGOD — CORNING
ALL CAPS — ERIE
ALL DIODES - FDG666 F'CHILD.
ALL JACKS #430 H. H. Smith

NO	REVISIONS
B	REV. ITEM 4 ADDED 4-82
A	RELEASE





NOTE:
SEE SHEET 2 FOR LOG FREQUENCY SCHEMATIC.

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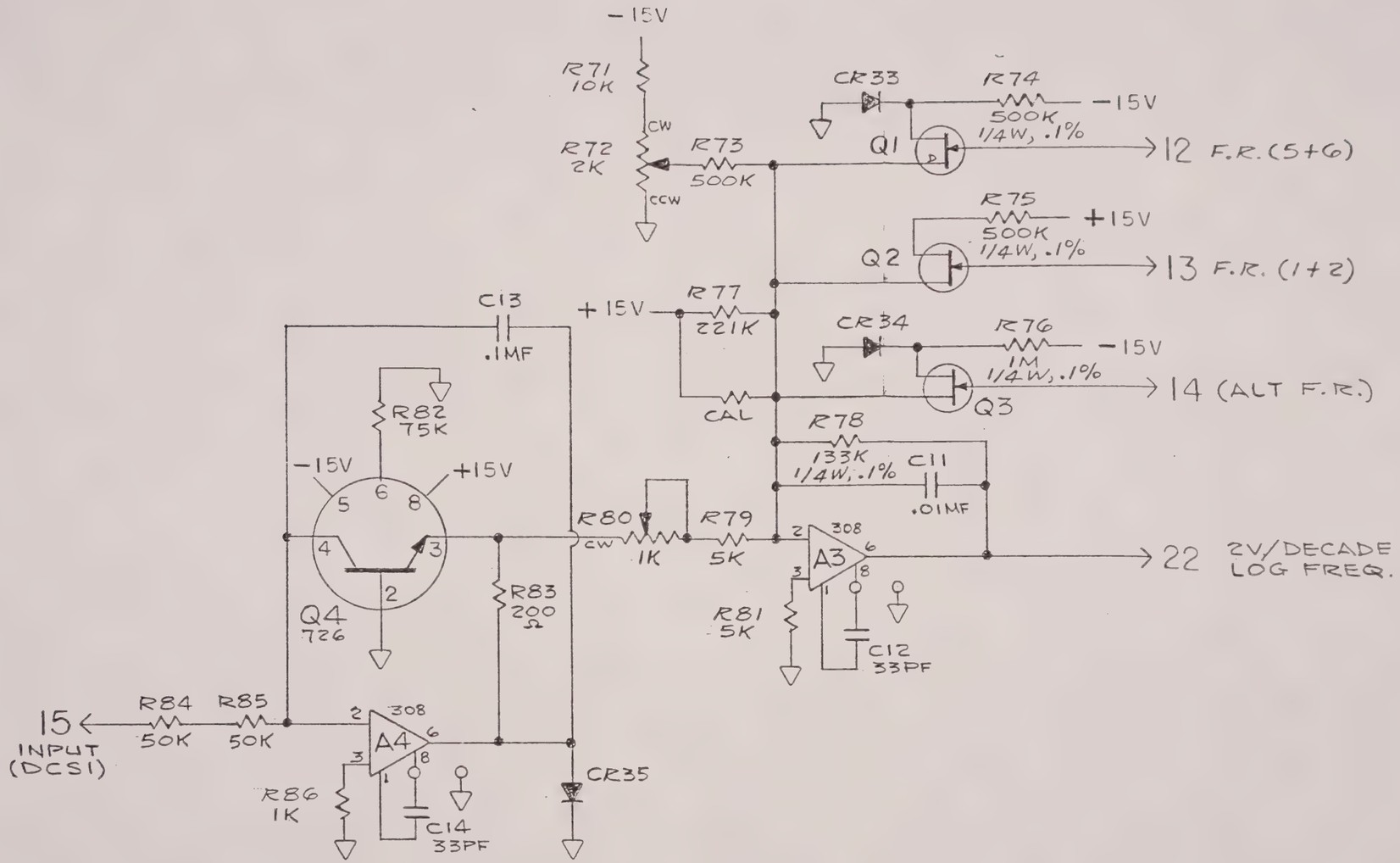
BAFCO, INC.

BAFCO, INC

BY Bezassi
DATE 25 MAR. '81
APPD
DATE

SCHEMA
COSINE G
MODEL 916



NOTE:
SEE SHEET 1 FOR PARTS LIST AND DESCRIPTION.

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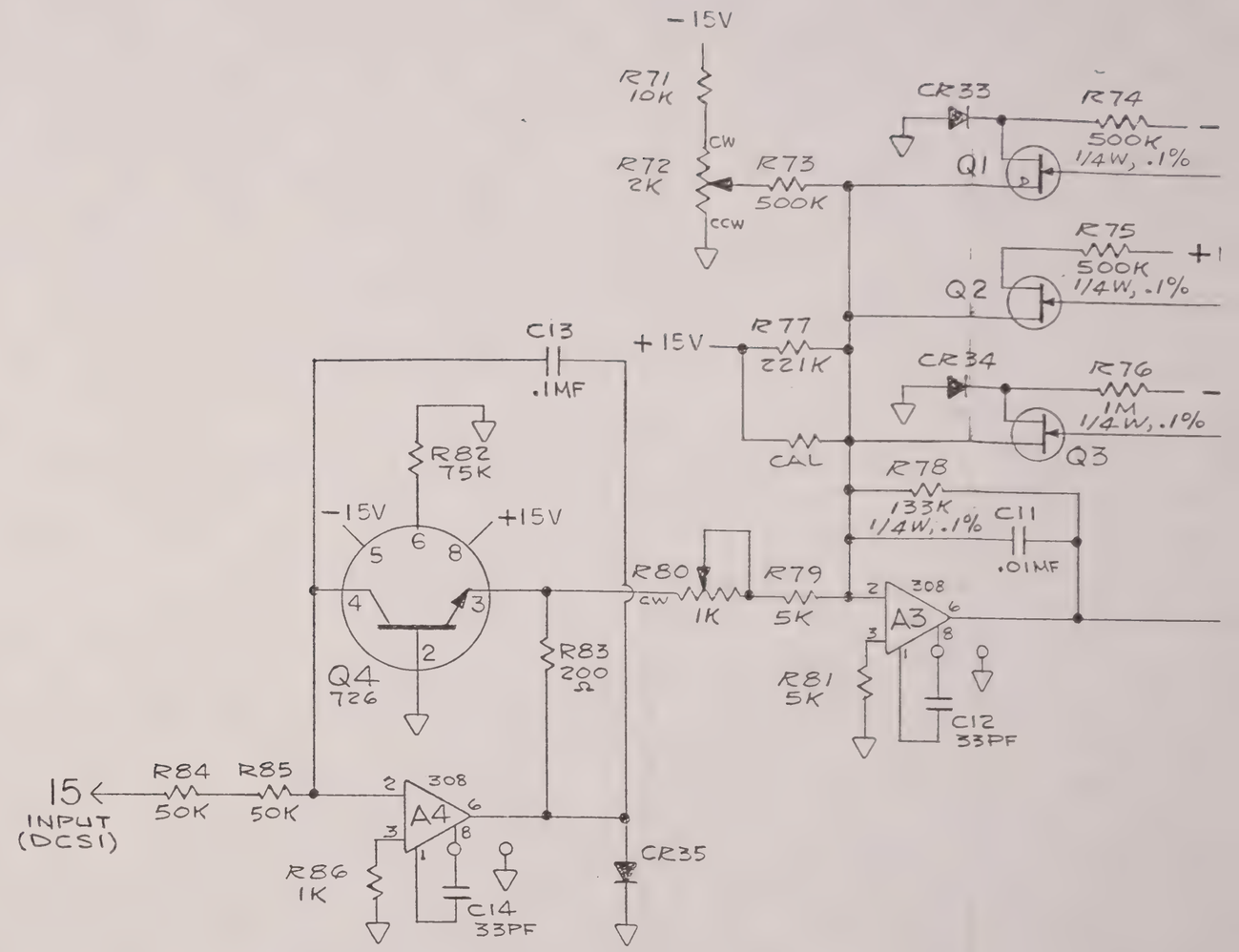
IT	Q	PT NO	DESC	VEND



NOTE:
SEE SHEET 1 FOR PARTS LIST AND DESCRIPTION.

NO	REVISIONS
B	REV. 4-82
A	RELEASE

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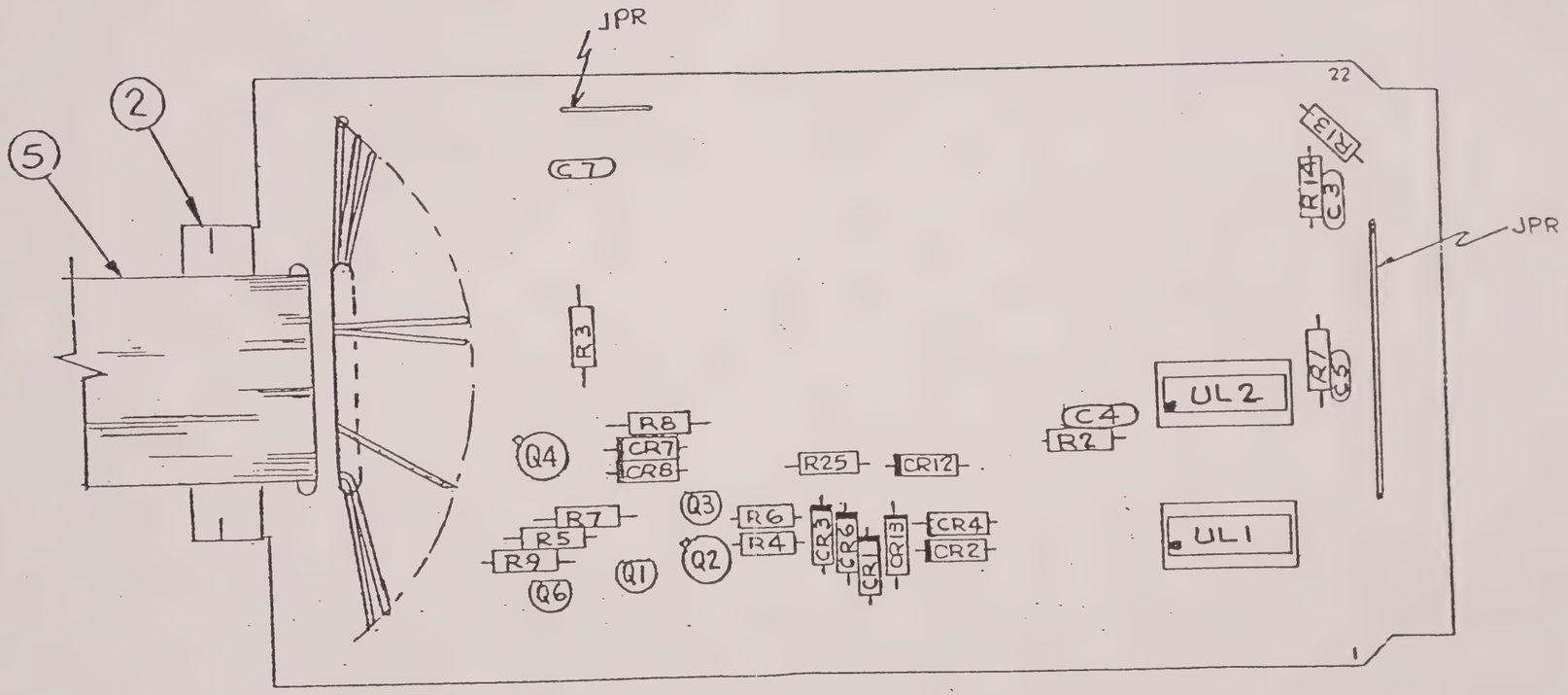
BAFCO, INC.

BAFCO, INC

BY [illegible]
DATE 25 MAR '81
APPD
DATE

SCHEMA
COSINE G
(WITH
MODEL 916X

REVISIONS			
NO	DESCRIPTION	BY	DATE
A	RELEASE		
B	REV.		5/79



UNLESS OTHERWISE SPECIFIED FRACTIONS ± .015 TWO PL. DEC. ± .010 THREE PL. DEC. ± .005 ANGLES ±1/2 DEG. SUR. FIN. 125 MICROINCH	THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	BAFCO, INC	ASSEMBLY R H. CABLE BOARD, P.C. MODEL 916H 916XH	BY GRASSI DATE 5-14-76 APPD DATE	B SCALE FULL 103548-A

NO	DESCRIPTION
A	RELEASE

ITEM	QTY.	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOR
1	1	103550		PRINTED CIRCUIT BOARD	BAFCO
2	1	100073		HANDLE	
3	2	516-AG-11D		I.C. SOCKET 16 PIN	AUGUT
4	—	514-AG-11D		I.C. SOCKET 14 PIN	
5	AR		#SS-4024=19B	CABLE - 24 GA.	SPECTRA
C1	—			C: .001MF	ERIE
C2	1			C: .01MF	
C3	1			C: .1MF	
C4	1			C: .1MF	
C5	1			C: .1MF	
C6	—			C: 470 PF	
C7	1			C: .1MF	
C8	—			C: 100 PF	
C9	—			C: 100 PF	ERIE
CR1	1		FD6666	DIODE	FAIRCHI
CR2	1				
CR3	1				
CR4	1				
CR6	1				
CR7	1				
CR8	1				
CR9	—		FD6666	DIODE	FAIRCHI
CR10	—				
CR11	1		IN5231	DIODE - ZENER	MOTOROL
CR12	1		FD6666	DIODE	FAIRCHI
CR13	1		FD6666	DIODE	FAIRCHI

PARTS LIST

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BAFCO, INC.

BAFCO, INC

ASSEMBLY
R.H. CABLE BOARD, P.C.
MODEL 916H

BY GRASSI
DATE 5/11/76

APPD
DATE

A

103549-A

REVISIONS		
NO	DESCRIPTION	
A	RELEASE	

ITEM	QTY	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOR
R1	1		RN60D	R: 20 Ω 1/4W. 1%	CORNING
R2	1			R: 20 Ω	
R3	1			R: 1.21K	
R4	1			R: 20K	
R5	1			R: 1.21K	
R6	1			R: 30.1K	
R7	1			R: 1.121K	
R8	1			R: 30.1K	
R9	1			R: 1.21K 1/4W. 1%	
R10	—			R: NOT USED	
R11	—			R: 20K 1/4W. 1%	
R12	—			R: 20K	
R13	1			R: 5K	
R14	1			R: 500 Ω	
R15	—			R: 8K	
R16	—			R: 2K 1/4W. 1%	
R17	—			R: NOT USED	
R18	—			R: NOT USED	
R19	—			R: NOT USED	
R20	—		RN60D	R: 10K 1/4W. 1%	CORNING
R21	1			R: 470 Ω 1/2W. 5%	AB
R22	—		RN60D	R: 20K 1/4W. 1%	CORNING
R23	—		RN60D	R: 20K 1/4W. 1%	CORNING
R24	1		RN60D	R: 2.5K 1/4W. .1%	CORNING
R25	1		RN60D	R: 30K 1/4W. .1%	CORNING

PARTS LIST

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BAFCO, INC.

BAFCO, INC

ASSEMBLY
R.H. CABLE BOARD
MODEL 916H

BY
DATE

APPD
DATE

A

103549-A

REVISIONS		
NO	DESCRIPTION	
A	RELEASE	

ITEM	QTY	BAFCO NO	VENDOR NO	DESCRIPTION	VENDOR
UL1	1		14028	I.C. 16 PIN	MOTOROLA
UL2	1		14049	I.C. 16 PIN	
UL3	—		14519	I.C. 16 PIN	
UL4	—		14553	I.C. 16 PIN	
UL5	—		14013	I.C. 14 PIN	
UL6	—		14528	I.C. 16 PIN	MOTOROLA
Q1	1		U1899E	TRANSISTOR	SILICONIX
Q2	1		2N5544	H.V. FET	TELEDYNE
Q3	1		U1899E	TRANSISTOR - FET	SILICONE
Q4	1		2N5544	H.V. FET	TELEDYN
Q6	1		U1899E	TRANSISTOR - FET	SILICONE
Q8	1		U1899E	TRANSISTOR - FET	SILICONE

PARTS LIST

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BAFCO, INC.

BAFCO, INC

ASSEMBLY
R.H. CABLE BOARD P.C.
MODEL 916H

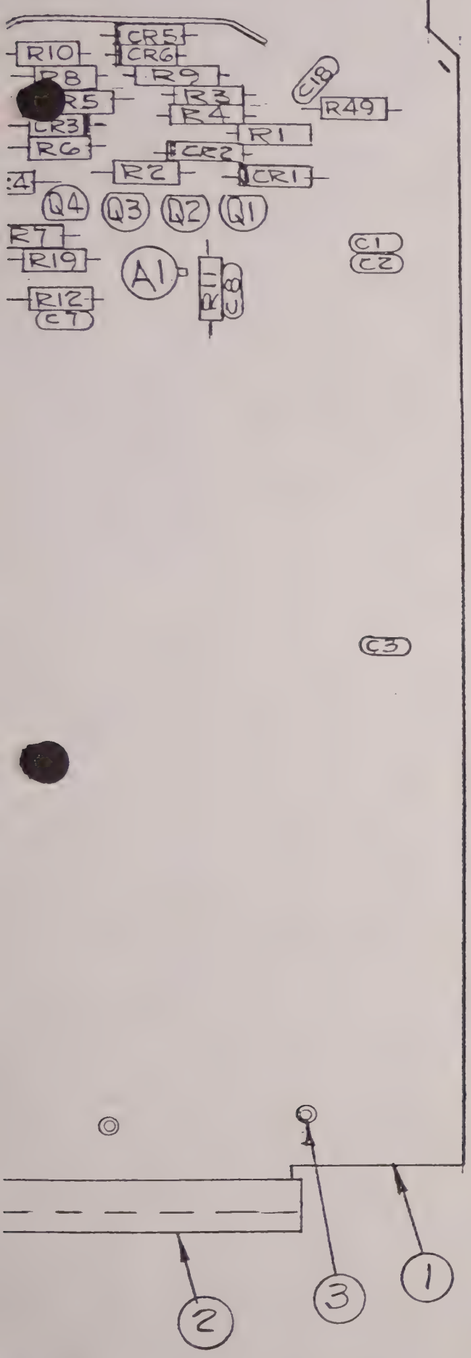
BY GRASSI
DATE 2/10/76

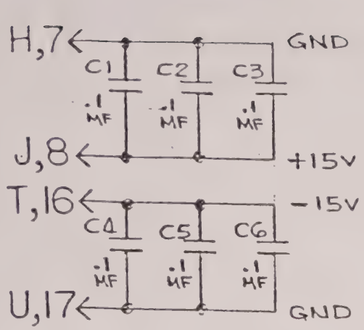
APPD
DATE

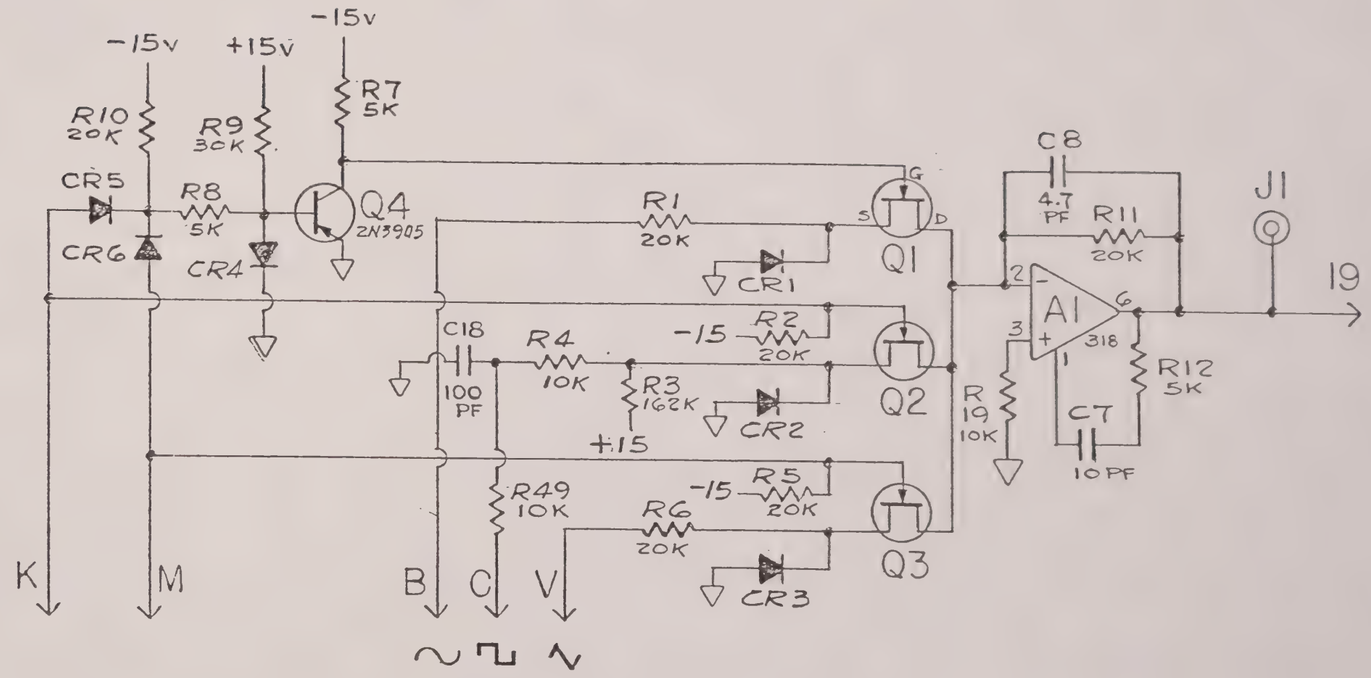
A

SH. 3 OF 3

103549-A







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BAFCO, INC.

BAFCO, INC

BY Grassi
DATE 8-23-76
APPD
DATE

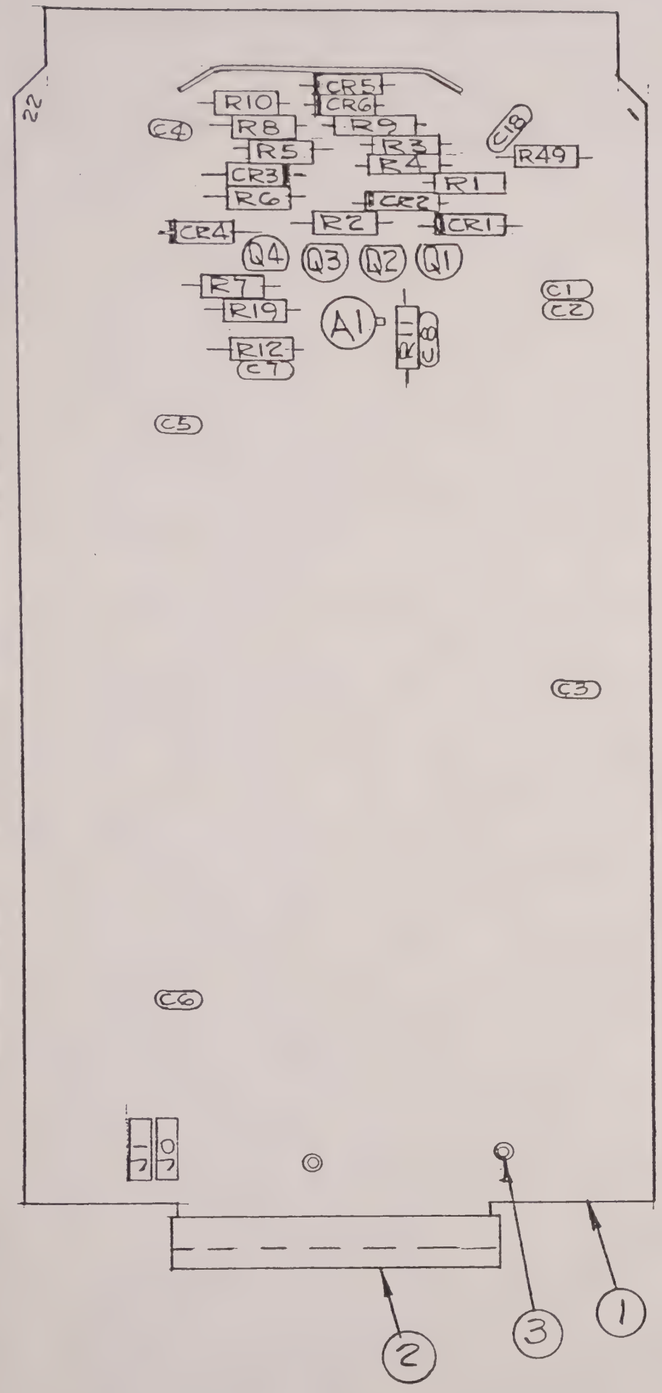
ASSEMBLY #6
SCHEMATIC – P.C. BOARD
PHASE TRIM & WAVE FORM SELECT
MODEL 916XH REF

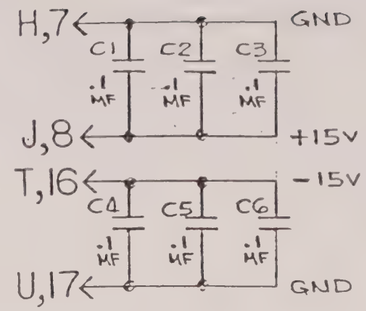
C

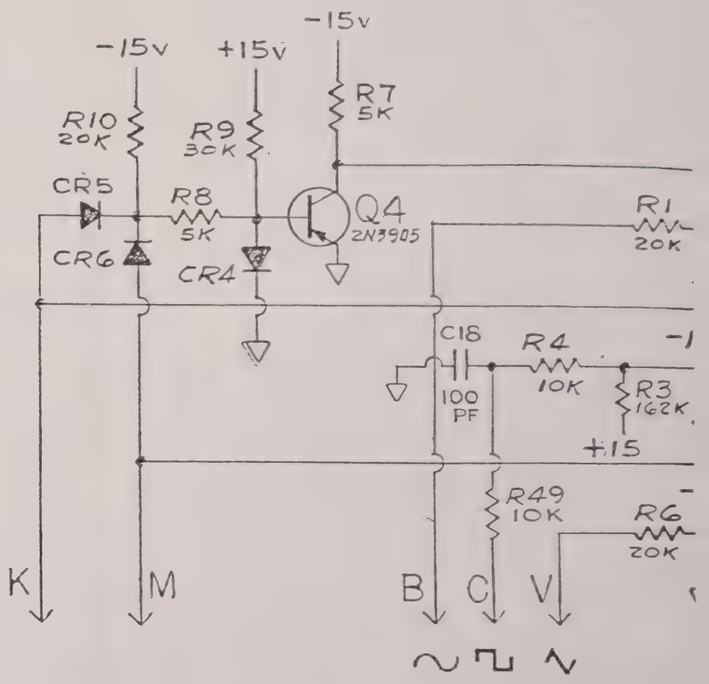
SCALE FULL

103634-12

1	103428	P.C. BOARD	BAFCO
1	100073	HANDLE	"
4R		TURRET LUG	CAMBION
1	LM318	AMPLIFIER	NAT'L.
1			
1	U1899E	TRANS. FET	SILICONIX
1			
1	2N3905	TRANS. PNP	MOT.







NOTES:
1-UNLESS OTHERWISE SPECIFIED
ALL RESISTORS 1/4W. 1%
RN60D — CORNING.
ALL CAPS — ERIE
ALL DIODES - FD6666
FAIRCHILD
ALL JACKS - #430 H.H.SMITH.

RELEASE	
REVISIONS	

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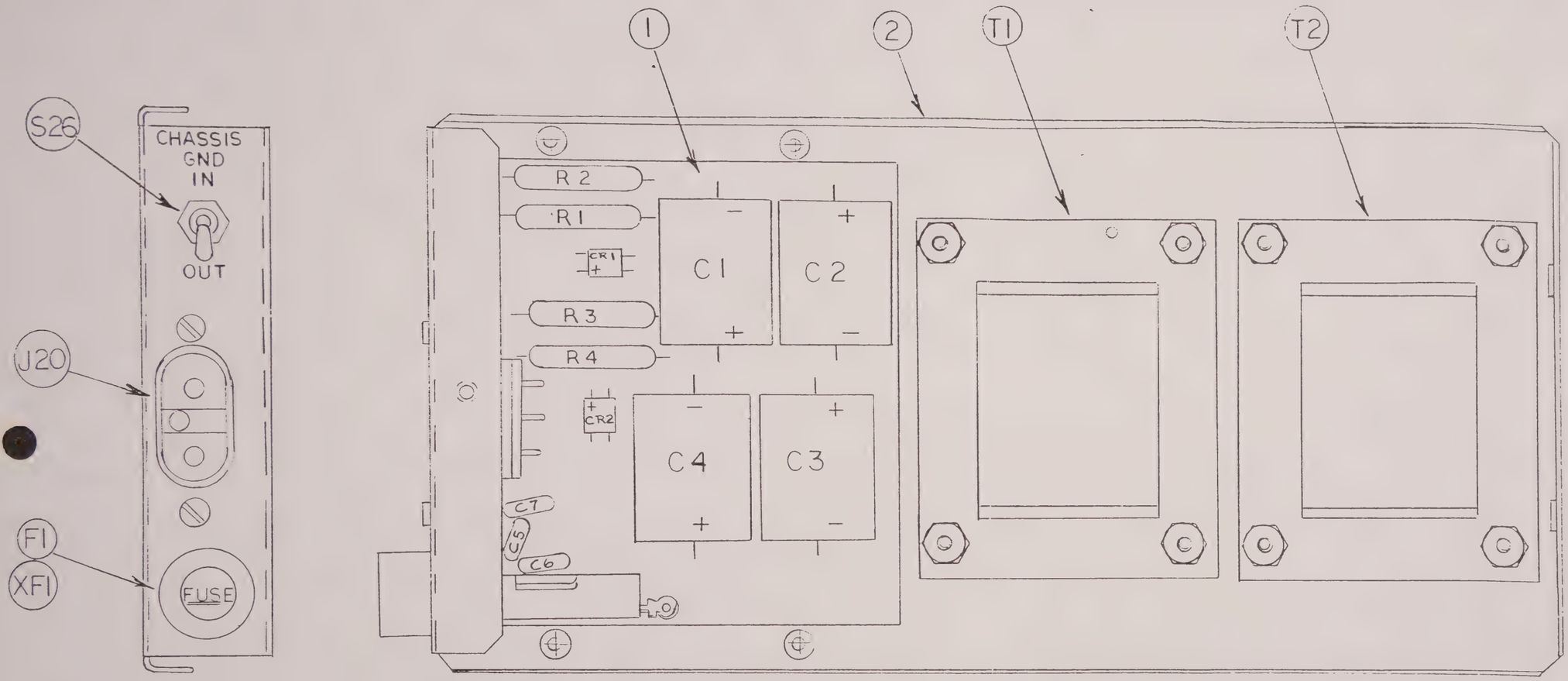
BAFCO, INC.

BAFCO, INC

BY [signature]
DATE 6-23-76
APPD
DATE

ASS
SCHEMA
PHASE TRIM
MODEL 916XH

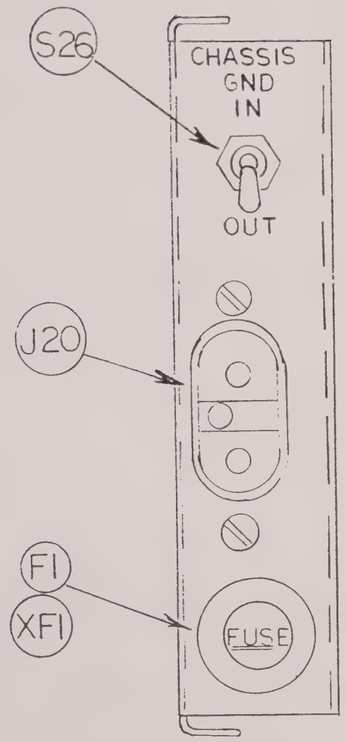


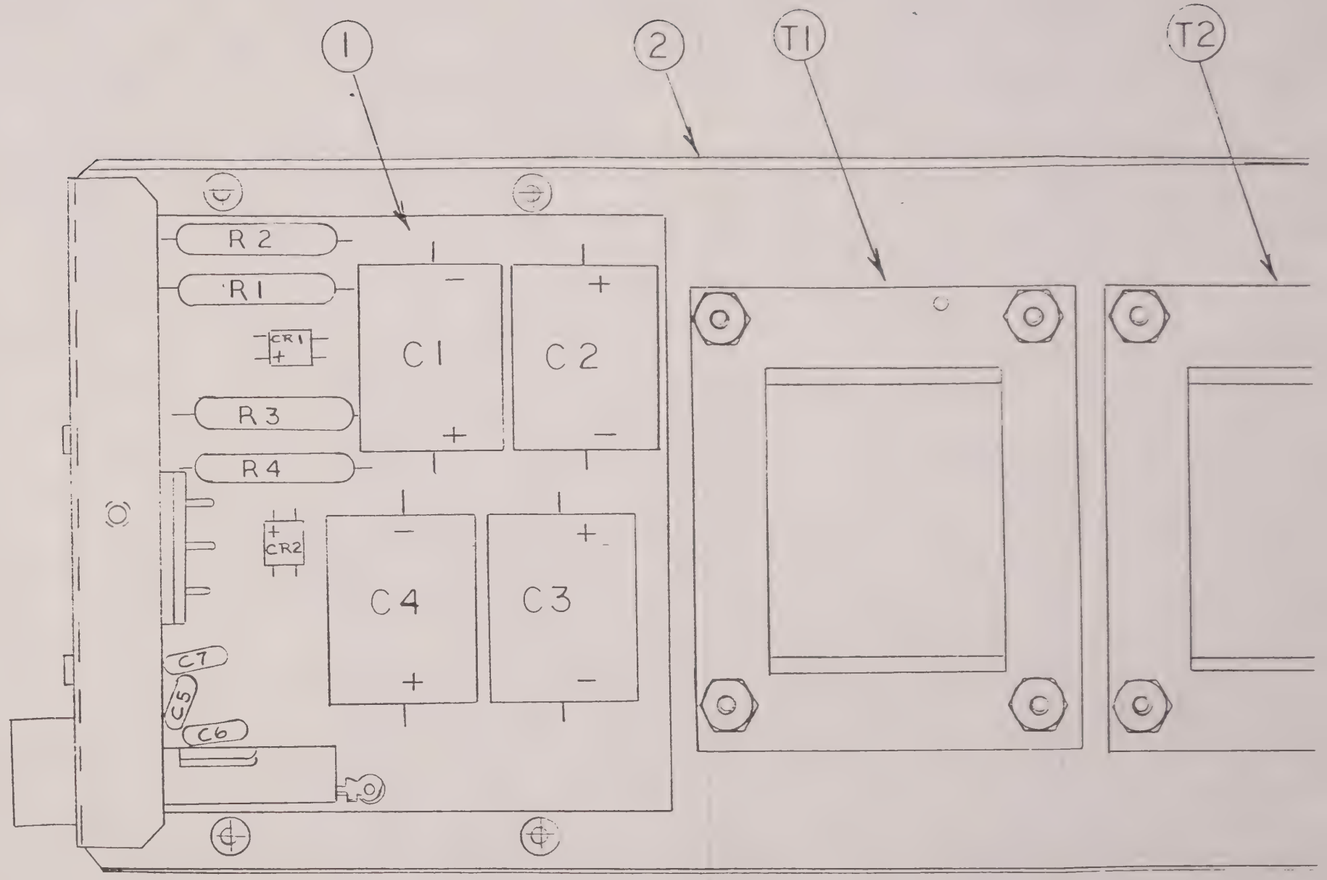
F2- PF127 FOR 110V & 220V
" PF127T 100 (100V)

REF. C103636

THE INFORMATION CONTAINED HEREIN IS THE PROPERTY OF BAFCO, INC. AND IS NOT TO BE USED EXCEPT AS AUTHORIZED IN WRITING. BAFCO, INC.	BAFCO, INC	BY SANDI DATE 2 APR '81 APPD DATE	ASSEMBLY DUAL RECTIFIER & FILTER (±15 V P.S.) MODEL 916H REF	C SCALE 103635

IT	Q	PT NO	DESC	VEND
1	1	1103636	DUAL RECT ASSY	BAFCO
2	1	B101426	P.S. TRAY	"
T1	1	SEE NOTE	XFMR	NTC
J20	1	AC3G	POWER RECPT.	SWITCHCRAFT
F1	1		FUSE 1 AMP.	LITTLE FUSE
XF1	1	341001	FUSE HOLDER	BUSSMAN
S26	1	7101MDZ	SWITCH - SPDT	C&K





NOTE:
* T1 & T2 - PF127 FOR 110V & 220V
" " PF127T 100 (100V)

NO	REVISIONS
C	REDRAWN 3-81 SS
B	REV. 12-77
A	RELEASE

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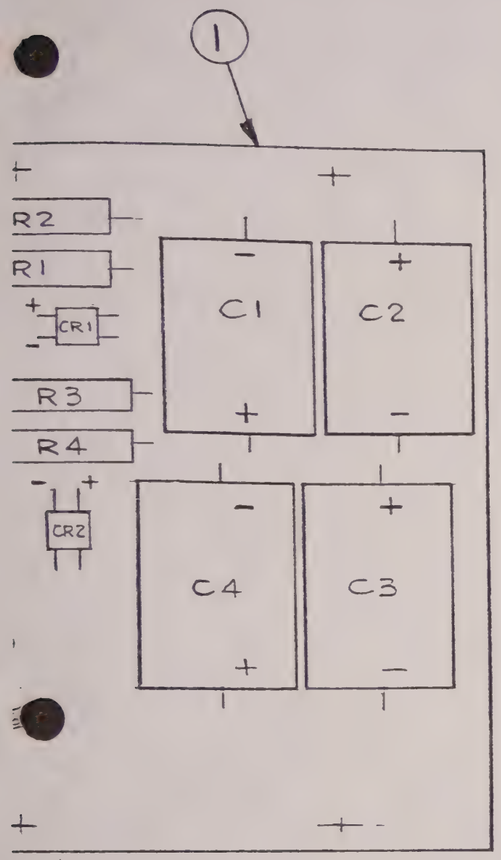
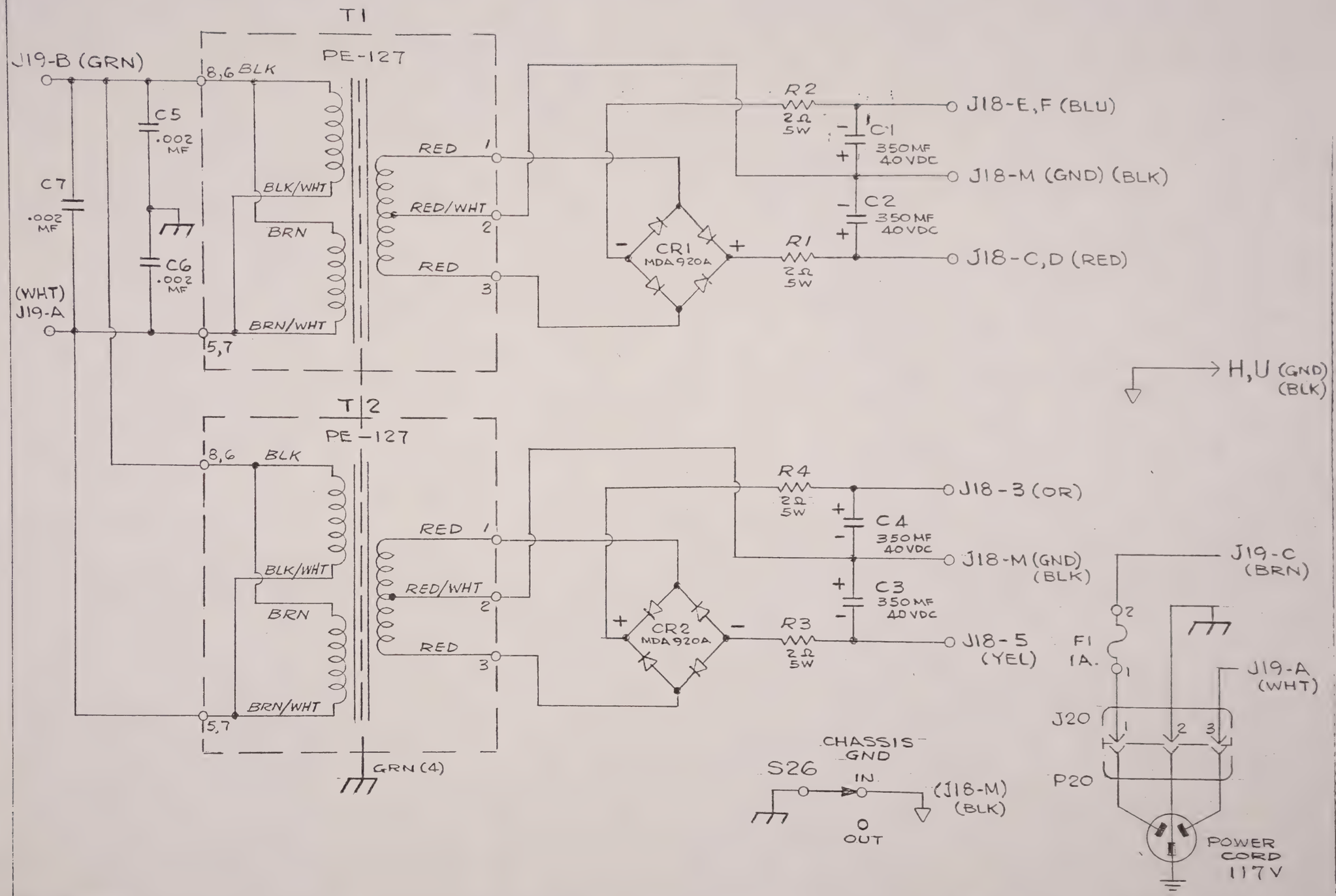
BAFCO, INC.

BAFCO, INC

BY SANDI
DATE 2 APR '81
APPD
DATE

A
DUAL RECTIFI
MODEL 916H





REF: 103635

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BAFCO, INC.

BAFCO, INC

BY DEASY
DATE 8-25-76
APPD
DATE

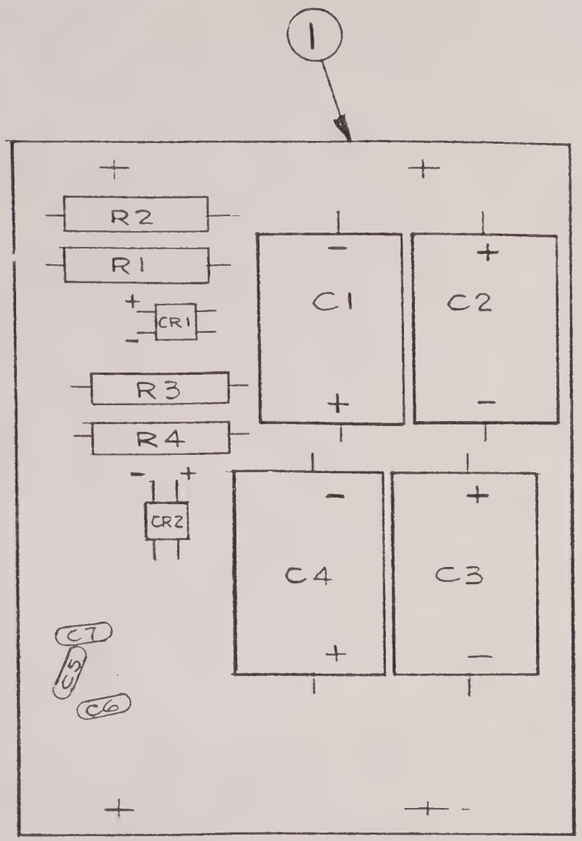
ASSEMBLY - SCHEMATIC
DUAL RECTIFIER & FILTER FOR DUAL ±15 VOLT REGULATOR

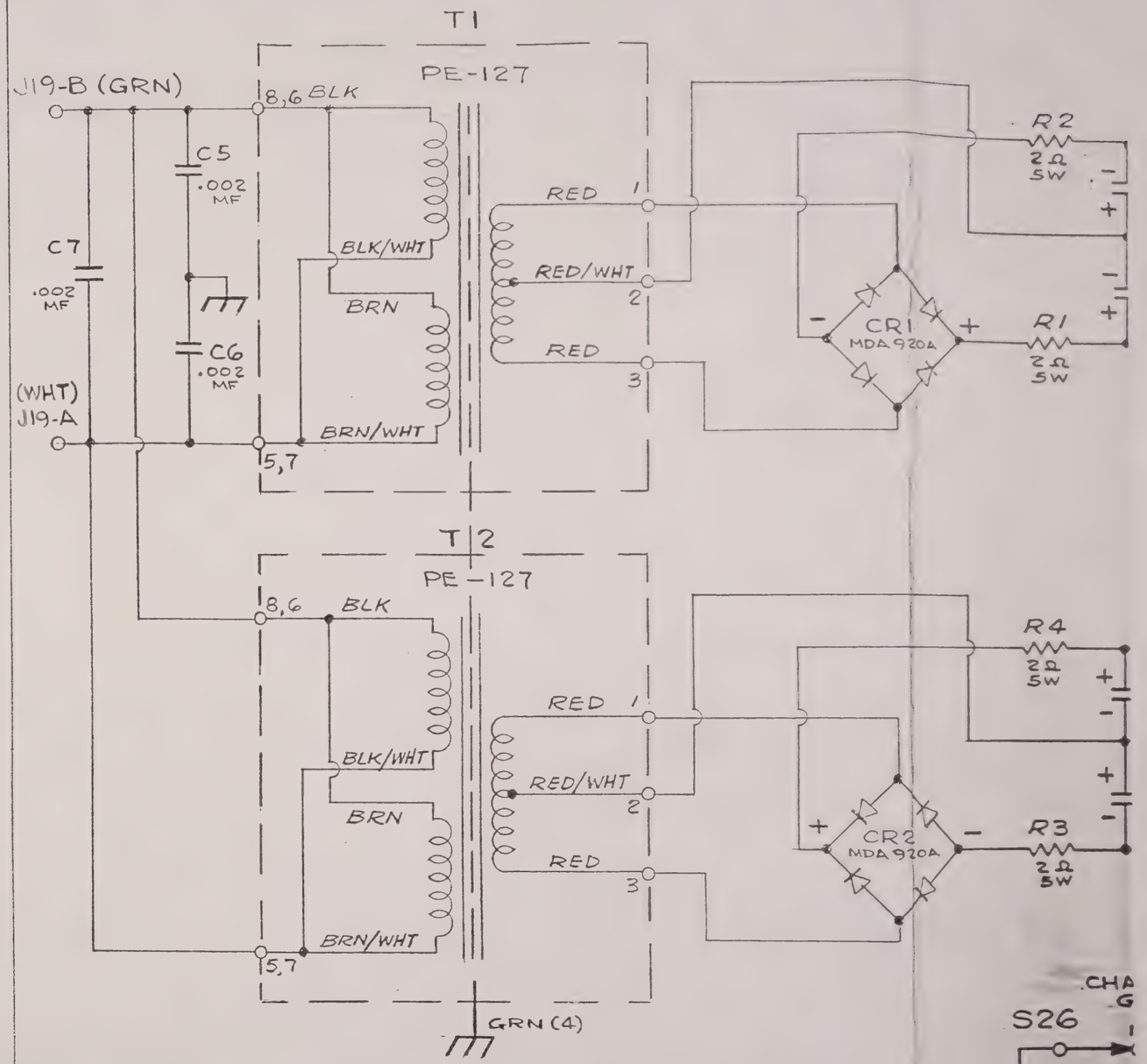
MODEL 916H REF

C | SCALE FULL

103636

IT	Q	PT NO	DESC	VEND
1	1	103621	P.C. BOARD	BAFCO
C2	1	#39D337 G0401E4	350MF @ 40VDC	SPRAGUE
C3	1			
C4	1			
R1	1	243EZR05	R: 2Ω 5W (WW)	SPRAGUE
R2	1			
R3	1			
R4	1			
CR1	1	MDA920A-3	RECTIFIER	MOTOROLA
CR2	1			
T1	1	PE127	TRANSFORMER	NTC
T2	1			





NO	REVISIONS
B	REV. WIRE COLOR ADDED 1-78
A	RELEASE

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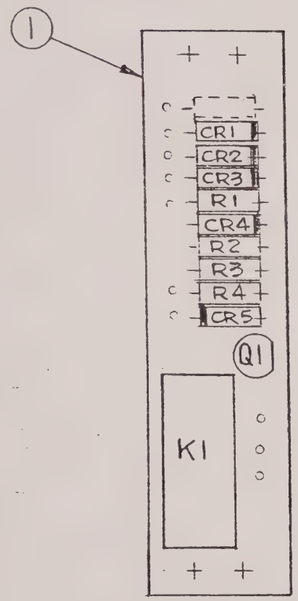
BAFCO, INC.

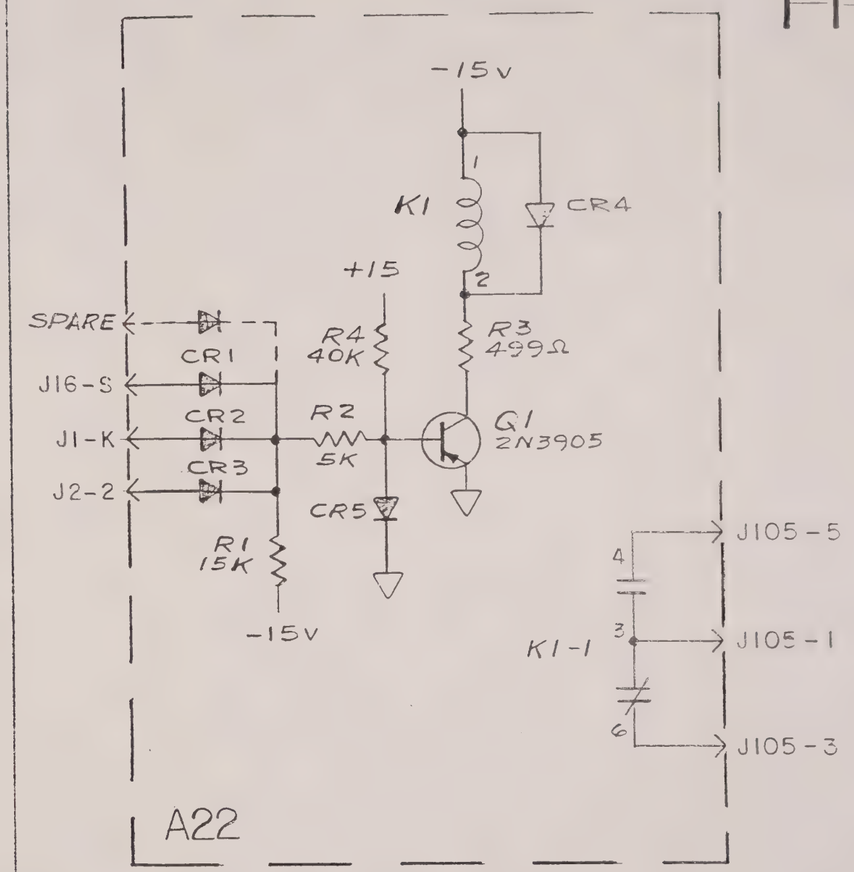
BAFCO, INC

BY [illegible]
DATE 8-25-76
APPD
DATE

AS
DUAL-RECTI
FOR DUAL
MODEL 916H

IT	Q	PT. NO.	DESC.	VEND
1	1	104103	P.C. BOARD	BAFCO
K1	1	MRB1C12	RELAY	CLARE
	1	2N3905	TRANSISTOR	MOT
R1	1		R: 15K 1/4W 1%	
R2	1	RN60D	R: 5K "	CORNING
R3	1		R: 499Ω "	
R4	1		R: 40K "	
CR1	1			
CR2	1			
CR3	1	FDG666	DIODE	F'CHILD
CR4	1			
CR5	1			





REVISIONS			
NO	DESCRIPTION	BY	DATE
A	RELEASE		
B	REV.		

UNLESS OTHERWISE SPECIFIED
FRACTIONS ± .015
TWO PL. DEC. ± .010
THREE PL. DEC. ± .005
ANGLES ± 1/2 DEG.
SUR. FIN. 125 MICROINCH

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BAFCO, INC.

BAFCO, INC

ASSEMBLY
SCHEMATIC - P.C. BOARD
AUTO PEN-LIFT
MODEL 916

BY GRASSI
DATE 3 JAN '79

APPD
DATE

B

SCALE FULL

104102

Choice of
0.85
Plastic
LED

AN2533/AN2553

UNIVERSAL, BIPOLAR ±3 1/2-DIGIT (±1999-COUNT) DIGITAL PANEL INSTRUMENT

The AN2533/AN2553 breakthrough instrument design reflects Analogic's world leadership in digital panel instrumentation . . . . . and the experience gained in producing more than 250,000 instruments.

Never before has the OEM user been offered so many and varied opportunities to incorporate "value-added" features into a digital panel instrument - - - increasing the profitability of his product, and exploiting fully his own design expertise. In fact, by standardizing on either of the two configurations, most OEM users can satisfy all of their 3 1/2 digit DPI requirements.

The AN2553 is the more versatile configuration. Its design includes an internal power and signal interface connector which accepts a general purpose plug-in card on which the user can install proprietary analog-interface circuitry. . . . . or Analogic can add the special purpose circuitry during manufacture, whichever is more economical. (Typical analog-interface functions that may be provided are: ac and dc current measurement, extended range ac and dc voltage measurement, active multipole filtering, information reinforcement filtering, thermocouple or RTD temperature transducer conditioning, LVDT excitation and demodulation, frequency-to-voltage conversion, current sourcing, auto-ranging, and ultra high impedance buffering.)

The AN2553 and AN2533 both provide power and space for an optional digital circuit card for such add-in features as isolated parallel BCD output, digital linearization, and set-point control. Here again, the add-ons may be provided by the user, or, for quantity requirements, engineered and built in by Analogic.

The AN2533 provides the same advanced performance features and inherent versatility of the AN2553, except that the analog-interface connector is omitted. The basic design common to both is so flexible and adaptable that this lower cost version provides far more value-added application freedom than any conventional design.

In either configuration, exceptional confidence in high quality and reliability is warranted by: (1) Application of worst-case error analysis to ensure specification integrity throughout rated life; (2) Minimizing the component count without "cornercutting;" (3) Exclusive use of premium, field-proven components; (4) 100% burn-in of all IC's; (5) Use of CMOS digital circuitry resulting in extremely low internal temperature rise (less than 10°C); (6) Generous derating margins; (7) 100% testing of subassemblies; (8) 4-day burn-in of all completed instruments **before** final test; and (9) Comprehensive, detailed quality-assurance procedures.

Design features that contribute to the wide-range versatility of this design include: a true symmetrical front end; dual-slope, long-period signal integration; choice of bright, luminous, 0.55" (14mm) gas plasma or 0.43" (11mm) LED display; common-mode rejection ratios up to 160dB; normal mode rejection ratios up to 100dB; and a universal 100/117/220/240 Vac power supply.

Compare 3 1/2-Digit Instruments - Study all available specifications. Consider this instrument's potential to maximize the value added to your product. We believe you will agree that we have made available the best general purpose DPI to fulfill present and foreseeable measurement needs.

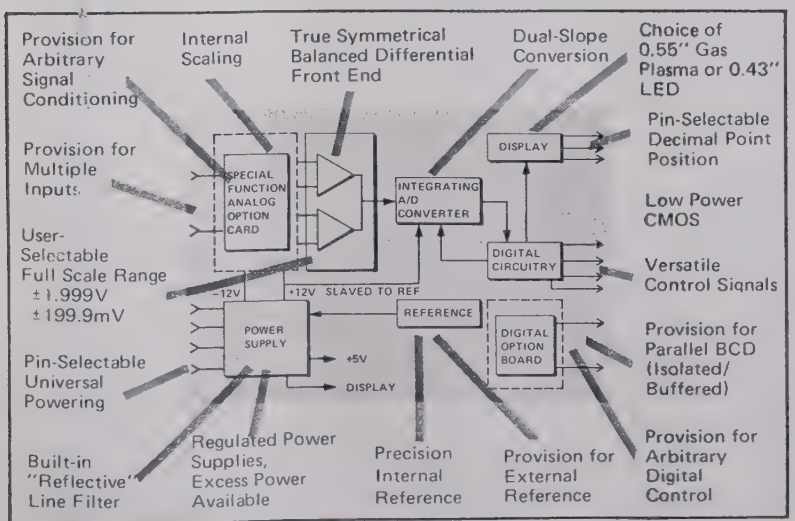


Figure 1. Simplified Block Diagram

FEATURES

- **ACCURACY AND STABILITY**
  Resolution: ±1999 counts
  Error: Less than ±0.05% Rdg ±1 count
  Noise: Deadband less than 0.1 count
  Temperature Coefficient: <35ppm/°C typical
- **DISPLAY OPTIONS**
  0.55" (14mm) gas plasma or 0.43" (11mm) LED, self-illuminating
  Automatic polarity
  Pin-selectable decimal points
  Dummy Zeros
- **UTMOST RELIABILITY**
  Low parts count; yet incorporating those needed for safe performance margins
  Cool operation:
  only 2 watts power consumption
  low-power CMOS circuitry
  Standard, proven, volume-production IC chips
- **USE-ORIENTED INPUT CONDITIONING**
  True-differential, balanced symmetrical inputs†
  Low bias current
  High input impedance
  Built-in signal offsetting capability
- **VERSATILE CONTROLS**
  External run/hold
  Remote display control
  User-selectable full scale range
- **UNIVERSAL POWERING**
  Universal transformer; pin connectable
  100, 117, 220 or 240Vac, 49 to 500Hz
  Highly regulated internal supply voltages;
  +5V, +12V, −12V with excess capability
- **PROVEN INTERFERENCE REJECTION**
  High CMRR & NMRR capabilities
  Built-in "reflective" line filter
- **ADAPTABLE MECHANICAL PROVISIONS**
  International DIN/NEMA standard case
  UL 94V-0 Rated
  Front-panel removeable, †easily serviced
- **WIDE ENVIRONMENTAL RANGE**
  Operating temperature range: −10°C to +60°C
  High rejection of electric fields
  Operational in harsh shock & vibration stresses
- **OEM INSTRUMENT-TO-PRODUCT TRANSFORMATIONS**
  By plug-in PC-board assemblies for thermocouple and RTD temperature indicators; pH meters; load cell, bridge, and LVDT weight, force, and pressure instrumentation; etc.
- **SYSTEM-COUPLING OF ANALOG INPUTS AND DIGITAL OUTPUTS**
  Low input bias currents:
  to fractions of picoamperes!
  Very high impedance input circuits:
  to 10^{12} ohms!
  Isolated and buffered parallel BCD outputs
  Power-sharing and coupling capabilities

†U.S. Patent numbers 3718923, 3751717, 3751791 and others pending

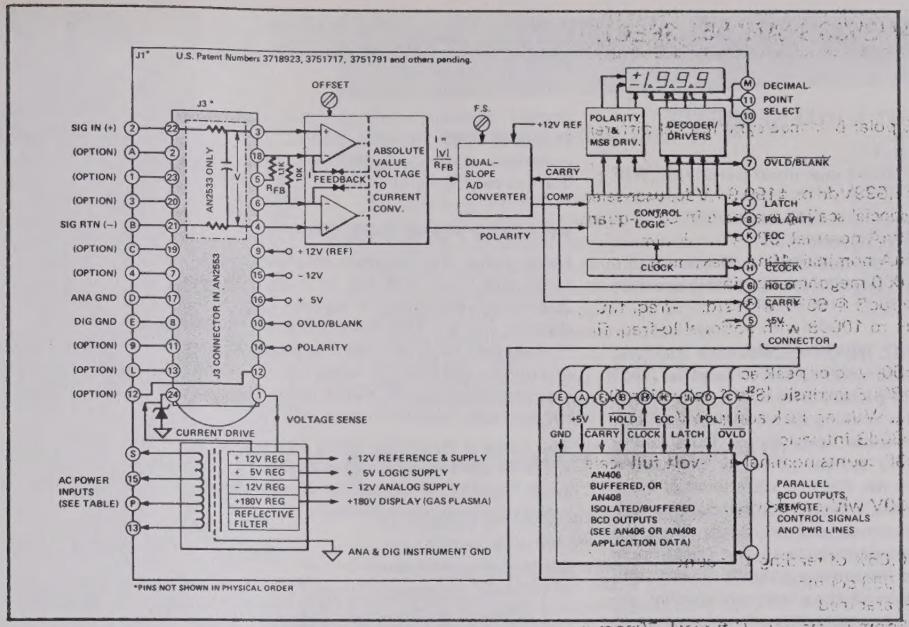
ANALOGIC®

. . . The Digitizers

AN2533 & AN2553 SPECIFICATIONS

		AN2553 EXPANSION CAPABILITIES
ANALOG INPUT		
Configuration	Bipolar balanced symmetrical differential inputs	Any arbitrary input transducer signal conditioning, plus filtering, amplifying, impedance-matching, and analog linearizing, etc.
Full-Scale Range	±1.999Vdc or ±199.9mVdc, user-selectable (special scaling available in OEM quantity)	Any arbitrary input signal scaling
Bias Current	10nA nominal, 30nA maximum	As low as 10^{-13} amperes
Offset Current	5nA nominal, 10nA maximum	As low as 10^{-13} amperes
Dynamic Input Impedance	1000 megohms nominal	As high as 10^{12} ohms
Normal Mode Rejection	>30dB @ 60Hz with std. hi-freq. filter; up to 100dB with optional lo-freq. filter	Up to 100dB
Common Mode Rejection		
Isolated Digital I/O: CMV Range:	±500Vdc or peak ac	
CMRR:	>80dB intrinsic (See Application Data)	Up to 160dB
Non-Isolated Digital I/O: CMV Range:	±2.5Vdc or peak ac-input V	
CMRR:	>80dB intrinsic	
Zero-Offsetting	±30 counts nominal at 1-volt full scale	Any arbitrary value consistent with maximum input voltage specifications
Maximum Differential Input Voltage	±20V without damage	Up to ±1000V without damage
ACCURACY/STABILITY		
Accuracy	±0.05% of reading ±1 count	
Resolution	±1999 counts	
Monotonicity	Guaranteed	
Range Tempco	35ppm of reading/°C typical, 70ppm of reading/°C maximum	
Offset Tempco	20μV/°C typical	
Recommended Recalibration Interval	12 months	
CONVERSION		
Technique	Dual-slope integration, each measurement independent of the previous measurement	
Control	Displayed conversion controlled by internal (clock) or external (arbitrary system-developed control logic) command (low level applied to Pin 6 of Connector J1)	Built-in, arbitrary system-developed control logic (See Application Data, page 4)
Rate	~2 readings/second (internal) or any lower rate controlled by external command	Any arbitrary rate less than 2 readings/second, controlled by built-in logic command (See Application Data, page 4)
Input Integration Period	100 milliseconds nominal	
DISPLAY		
Type	7-segment gas plasma 0.55" (14mm) or LED 0.43" (11mm), planar	
Number of Digits	3 full-decade digits, and "1" in most significant digit position (See Ordering Guide, page 3 and Fig. 11, for dummy zero options.)	
Decimal Point	Externally programmable in three positions (See Application Data, page 4)	
Polarity	Automatic, plus or minus sign displayed	
Overload (More than 1999 Counts)	All digits blanked; polarity and decimal point remain lighted	
DIGITAL SIGNALS (See Timing Diagram, Figure 3.)		
Logic Levels (All Inputs and Outputs)	DTL/TTL/CMOS compatible. Sinks 1.6mA at low level (0 to 0.5V) and sources 40μA at high level (+3.5 ±1V)	
External Blanking	Low level input (on Pin 7) blanks three least significant digits	
Hold	Low level input (on Pin 6) retains last reading in display (See Figure 7.)	
Overload	Low level output (on Pin 7) indicates a measurement greater than 1999 counts	
Clock	Continuous (100kHz nominal)	
Latch	High level output (on Pin J) indicates that counter contents are being transferred into latches	
Carry	Rising edge (on Pin F) indicates counter carry (See Application Data)	
EOC	Rising edge (on Pin K) signals end of conversion (EOC)	
Polarity	High logic level (on Pin 8) indicates measurement is negative	
BCD OPTION CARDS	Isolated and/or buffered parallel BCD outputs (See Application Data).	
MTBF	43,000 hours calculated	
POWER		
Input Voltage	100, 117, 220, or 240Vac rms ±10%, 49 to 500Hz	
Available Output Voltage	+4.75Vdc ±5% at 30mA +12Vdc ±8% at 10mA; −12Vdc ±8% at 10mA	
Consumption	2 watts nominal*	
ENVIRONMENTAL & PHYSICAL		
Operating Temperature	−10°C to +60°C (+14°F to +140°F)	
Storage Temperature	−25°C to +85°C (−13°F to +185°F)	
Relative Humidity	0 to 95%, noncondensing	
Weight	12 ounces nominal (340 grams)	
Case	High-impact molded plastic case UL 94V-0 Rated standard; metal case available as an option	
Dimensions	DIN-Standard: 96mm (3.78 inches) bezel width x 48mm (1.89 inches) bezel height x 104.9mm (4.13 inches) max. depth (see Figure 8)	

*Slightly higher with LED displays



Pin Designations

J1 (bottom)

ANA OPT[1]	A	1	ANA OPT[1]
SIG RTN (–)[2]	B	2	SIG INPUT (+)[2]
ANA OPT[1]	C	3	ANA OPT[1]
ANA GND	D	4	ANA OPT[1]
DIG GND	E	5	+5V OUT
CARRY	F	6	HOLD
CLOCK	H	7	BLANK IN/OVLD OUT
LATCH	J	8	POLARITY
EOC	K	9	DIG OPT[1]
DIG OPT[1]	L	10	DEC PT 1
DEC PT 3	M	11	DEC PT 2
DIG OPT[1]	N	12	DIG OPT[1]
AC LINE[3]	P	13	AC LINE[3]
DIG OPT[1]	R	14	DIG OPT[1]
AC LINE[3]	S	15	AC LINE[3]

[1] In AN2553, available for user selection with Special-Function card.
[2] AN2533 connection as shown. In AN2553, available for user selection with Special-Function card.
[3] See Table below for powering selection.

TRANSFORMER CONNECTIONS

LINE VOLTAGE*	P	13	S	15
100V	●			●
117V (120)	●		●	
220V		●		●
237V (240)		●	●	

*49 to 500Hz.

Figure 2. Functional Block Diagram

Operating Features & Principles of Operation

As shown in Figure 2, the AN2533 contains a balanced signal enhancement input filter; a floating true differential front end; an absolute-voltage-to-current converter; a dual-slope ratiometric, current-to-count integrating analog-to-digital converter; clock-driven logic control circuitry, decoders, drivers and displays; and regulated power supplies derived from the secondary windings of a universal transformer.

Signal input to connector J1 is conditioned by the built-in filter (AN2533) or by arbitrary signal conditioning on the analog option card inserted in internal connector J3 (AN2553), resulting in a potential difference (V) at J3, pins 3 and 4, connected to the non-inverting inputs of the differential input amplifiers. The conditioned signal input (V) develops a unidirectional signal current (I), whose magnitude depends on the value of the selected feedback resistance (R_{FB}), according to the simple Ohm's Law formula shown in Figure 2. The signal current linearly charges a high quality, low leakage, integrating capacitor during the signal integration phase of the dual slope conversion. The current generation circuitry also includes the polarity sensing for display.

Under control of the 100kHz clock-driven logic, the signal integration phase lasts 10,000 counts, thus adding to the overall signal enhancement by providing very high rejection of normal mode interfering noise. At the end of the 10,000 counts, the $\overline{\text{CARRY}}$ control signal causes the integrator to switch into the reference integration phase, during which the integrating capacitor is discharged at a constant rate determined by a current derived from the precision +12V reference until the comparator changes state. The precision resistor network determining the integrating reference current is mounted on the same substrate as the built-in selectable feedback resistance (R_{FB}). Thus maximum thermal tracking of ratio-determining dual-slope performance components is obtained. This contributes to the exceptional overall thermal stability of the conversion. Moreover, because the signal integration phase is at least 5 times as long as the reference integration phase (10,000 counts to a maximum of 2,000 counts), noise disturbances are reduced significantly in the output.

The count accumulated during the reference integration phase is latched into the storage register, decoded, and, in addition to the polarity sensed in the current generator, used to update the display about twice a second for optimal flicker-free readings. When the count exceeds 1999, the Control Logic generates an overload (OVLD) signal which blanks the decimal digits while leaving the polarity sign and the selected decimal point lighted.

In addition to decimal point programming, the user may blank the least three significant digits or may choose to hold a displayed conversion by applying DTL-compatible signals at the designated terminals of J1. It is of interest to note that the instrument continues to update its digitized measurement, making available a valid display after the HOLD signal is released.

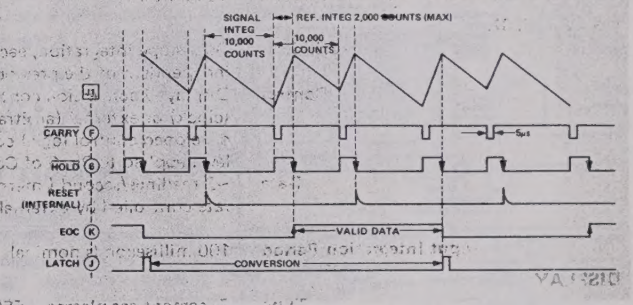


Figure 3. Timing Diagram

DTL/TTL-compatible digital output signals of LATCH, CARRY, EOC, HOLD, and CLOCK, as well as the OVLD and POLARITY signals, are available at connector J1, and are related to the charge-discharge cycle of the integrating capacitor as shown in the timing diagram of Figure 3.

Analog Function Card

Connector J3, when utilized, brings to the analog function card a number of input signal connections, as shown, and all power sources and their ground return references for use in such signal conditioning circuits as described in the Application Data.

Digital Function Card

There is an excess of +5V to power the snap-in digital option card on which isolated and/or buffered BCD outputs are generated. Connections are made via the standard panel instrument connectors. (See Application Data, page 6.)

ORDERING GUIDE

Simply Specify ——— [ ] – [ ] – [ ] – [ ]

Universal Digital Panel Instrument	AN2533
Expanded Digital Panel Instrument	AN2553
Gas Plasma Display	S
LED Display	L
UL 94V-0 Rated Plastic DIN/NEMA Case (Order PL10-5563 Connector)*	P
Extruded Aluminum DIN/NEMA Case (Order PL10-5563 Connector)*	M
One Dummy Zero (LED Only)	1DZL
Two Dummy Zeros (LED Only)	2DZL

*Optional Screw-Terminal Connector (Analogic PL10-5535) available for solderless wiring for plastic or metal case (See Figure 9)

INPUT SIGNAL ENHANCEMENT & INTERFERENCE REJECTION

The AN2533/AN2553 exceptional overall signal interference rejection is a combination of:

(1) The intrinsic front end (input terminal related) CMR
(2) The normal mode input filter rejection, and
(3) The long-time integration in the dual slope A/D converter.

As a result, the user has a remarkable flexibility in obtaining accurate normal mode (series) noise rejection.

TRUE, BALANCED, DIFFERENTIAL INPUT & CMR

The very high impedance, true balanced symmetrical differential front end (not to be confused with some pseudo-differential types) provides the user with the versatility for making direct additive or subtractive measurements of local or remote noisy inputs from one or more sources, referenced to arbitrary system power or instrument ground. The digitized output represents the true difference of input potentials, and, therefore, it is insensitive (see specifications) to voltage variations and fluctuations common to both terminals. Thus, the input differential circuitry itself can contribute to the rejection of common mode potentials referred to instrument ground. In addition, because of the high degree of isolation of the power transformer, excellent rejection ratios are achieved for common mode voltages up to ±350V with respect to power line ground.

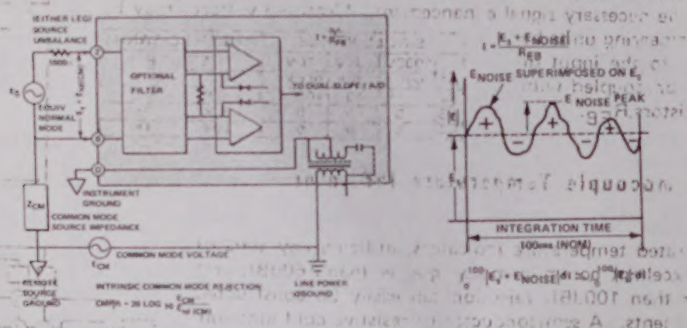


Figure 4. Transformation of Common Mode Signals, E_{CM}, to Normal Mode Signals, $E_{td(CM)}$, NMR, and Rejection by Integration

NORMAL MODE REJECTION

Normal mode interference signals, resulting either from conversion of common mode voltage to differential voltage or from additive (series) interferences, may be filtered out by a combination of passive or active input filtering and conversion integration. The standard DPI (see specs) is supplied with a nominal 20Hz low pass single-pole filter which, in combination with the integration effect, yields approximately 30dB rejection at 50/60Hz. There is ample provision within the AN2533/53 to incorporate either lower frequency and multipole passive filters and/or active filters which utilize the input differential amplifiers as their active elements (see Example A, page 5), so as to obtain normal mode rejections up to 100dB or greater at 50/60Hz.

INTERFERENCE REJECTION BY INTEGRATION

Remaining interference components (after front-end terminal related and input filter rejection) are still further reduced by the 100ms integration. For net signal level-to-peak noise ratios higher than one, the bipolar integration is complete so that, even for non-synchronous 50 or 60Hz interference, rejection greater than 20dB will be achieved.

Overall common mode rejection ratios of greater than 160dB (for example, 80dB intrinsic CMRR, +60dB NMRR, +20dB integration rejection) at 50 or 60Hz with 1000 ohm unbalance in either input line can readily be obtained!

ANALOG FUNCTION CARD

Using either the Analogic AN450 General Purpose Analog Function Card with Filter (see Fig. 11), which is typically capable of handling 30 arbitrary components, including potentiometers, dual in-line ICs, and discrete 2-and 3-lead components, or by designing his own such card, the user may build in proprietary circuitry for any arbitrary signal conditioning, excitation, or linearizing function, utilizing the available excess regulated power, stable reference, and additional input terminals for optimum system compatibility.

The General Purpose Analog Function (kluge) Card, with a pre-engineered layout for optimum component space utilization, is held securely in the DPI by connector J3 and the case without the need for any additional mounting hardware.

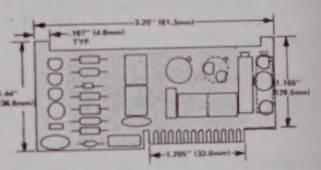


Figure 5. Typical Kluge Card Layout

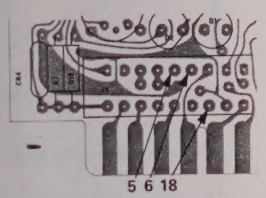


Figure 6. PC-Board Scaling Connections

ARBITRARY SCALING

With a 10,000Ω feedback resistor (R_{FB}) connected as shown in Figure 2, the DPI is normally calibrated at the factory for a full-scale range of 1 volt/1,000 counts. A thermally tracking internal resistor, 1.1kilohms, may be connected in parallel with the 10,000 ohm resistor by a jumper between positions 5 and 6 on the main assembly PC board (AN2533) or by connections on the analog option board (AN2553). The parallel resistance of 1,000 ohms provides the user-selectable sensitivity of 100mV/1,000 counts (100μV/count). Any other sensitivity may be obtained by a net resistance between positions 6 and 18 according to the formula $R = \frac{\text{Voltage/1,000 Counts}}{0.1\text{mA}}$.

HOLD

To hold a displayed reading, gate a HOLD command (the comparator output shown in Figure 2) with the rising edge of EOC (available at pin K), and then generate a DTL low level signal (HOLD). When applied to Pin 6 of the DPI connector, the HOLD signal will keep the last conversion displayed, while the DPI continues to update the measurement internally. When HOLD is removed, the next valid measurement is transferred to the display latches.

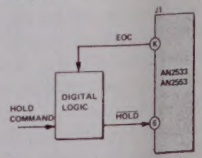


Figure 7. Generating a Hold Command

ANALOGIC LIBRARY OF SPECIAL FUNCTION CARDS

DIGITAL CIRCUIT OPTIONS

AN404 Function PC Card DIN Standard
AN406 Latched, Buffered Parallel BCD Output Card
AN408 Isolated, Buffered Parallel BCD Output Card

ANALOG CIRCUIT OPTIONS

AN450 Analog Function PC Card with Input Filter
AN451 Analog Function PC Card without Input Filter
AN452 Thermocouple Cold-Junction Compensation Card
AN453 RTD Temperature Card
AN454 Input Filter Card
AN455 Industrial Current Receiver Card
AN456 Industrial Voltage Receiver Card
AN461 True RMS AC Voltmeter Card
AN462 Power Line Voltage Monitor Card
AN463 Microvolt Receiver Card
AN466 Linearized Thermocouple Card

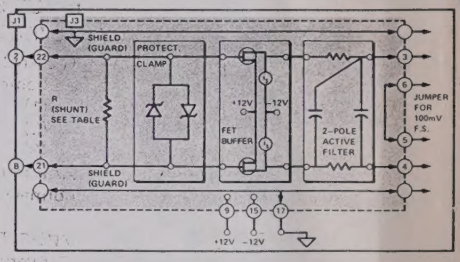
APPLICATION DATA

The examples below are only a few of the essentially limitless applications of the AN2553. Th indicate the wide range of applications, versatility, and ease of using this digital panel instrument.

Assemble A Precision Current Meter

F.S. RANGE	UNIT COUNT	SHUNT, R
2.000 Amp	1mA	0.100Ω
200.0mA	100µA	1.000Ω
20.00mA	10µA	10.00Ω
2.000mA	1µA	100.0Ω
200.0µA	100nA	1.000KΩ
20.00µA	10nA	10.00KΩ
2.000µA	1nA	100.0KΩ
200.0nA	100pA	1.000MΩ
20.00nA	10pA	10.00MΩ
2.000nA	1pA	100.0MΩ

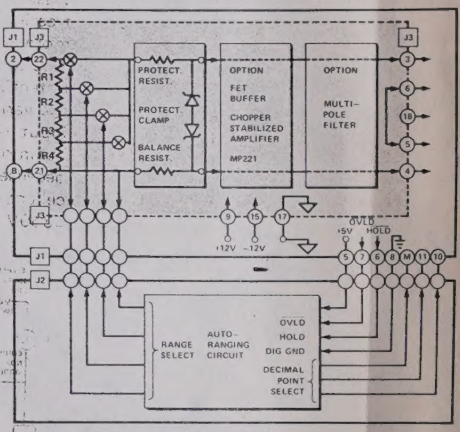
To measure current from amperes to picoamperes, simply select the standard 100mV/1,000 count DPI sensitivity and install the appropriate shunt resistance. Depending on the signal amplitudes and interferences, design protective clamps, low leakage FET buffers, and multipole filters. Appropriately guard for higher sensitivity operation by eliminating leakage current paths. Digitize the output in any arbitrary engineering units by modifying the shunt resistance between Pins 6 and 18 of J3. By connecting either end of the shunt to analog ground, or by other means, assure circuit conformance to common mode limits.



Build An Extended Range Voltmeter

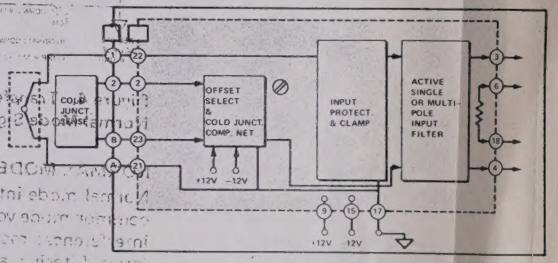
To measure any voltage from kilovolts to microvolts, use either of the selectable standard DPI sensitivities and the appropriate voltage divider network. Depending upon whether a single-range or multiple-range voltmeter is desired, design suitable switching circuits to be activated either by externally programmed range select signals, or optionally, by range control signals developed on the digital function card. Protect the input circuitry with resistive and clamping components, and introduce an optional FET buffer, chopper stabilized amplifier, or standard amplifier module such as the Analogic MP221 if needed in very low level signal applications. Incorporate an optimal filter to obtain the necessary signal enhancement. Measured voltages may be scaled in arbitrary engineering units by suitable modifications to the input divider network alone, or coupled with appropriate scaling resistors, R_{FB}.

	SINGLE-RANGE			MULTIPLE-RANGE	
	1000V	100V	10V	EITHER	
R1	999K	990K	900K	9M	900K
R2	1K	10K	100K	900K	90K
R3	0	0	0	90K	9K
R4	0	0	0	10K	1K



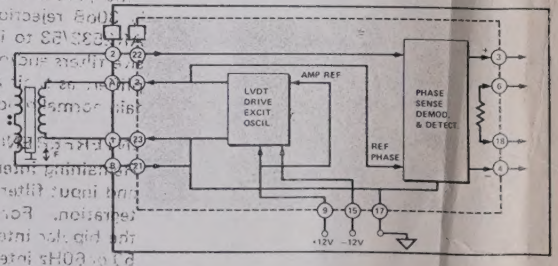
Construct A Thermocouple Temperature Indicator

Cold-junction-compensated temperature indicators, utilizing any type of thermocouple, with excellent common mode (greater than 160dB!) and normal mode (greater than 100dB!) rejection can easily be constructed with just a few components. A semiconductor or resistive cold junction sensing element, stably powered by the DPI +12V power reference, can generate an offset and cold-junction compensation variable voltage which can be directly subtracted (or added) from the thermocouple-developed voltage via the true differential balanced input circuitry. Input resistor and zener clamps may provide protection, and filter components as shown in "A" above may form an active two-pole filter. The appropriate resistor across Pins 6 and 18 of J3 scales the output directly in temperature-related engineering units.



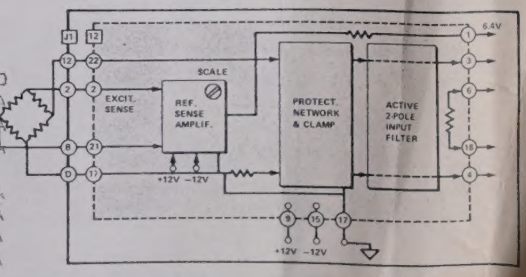
Develop An LVDT Position Or Force Indicator

The excitation winding of an LVDT may be driven over a wide range of frequencies by an excitation oscillator powered by the ±12V regulated supplies and amplitude regulated by the precision +12V supply. The combined differential winding output of the LVDT can then be phase sensitive demodulated in a simple switching circuit whose phase reference is derived from the excitation oscillator. The filter output of the phase sensitive demodulator can then be applied directly to the differential inputs of the DPI. Again, the output may be scaled in any desired force or linear units by choosing the appropriate resistor across Pins 6 and 18 of J3.



Engineer A Ratiometric Load Cell Meter

The ratiometric capability of the AN2533/2553 may be exploited to perform ratiometric measurements of bridge transducer outputs with an accuracy independent of the external excitation supply variations. Available input pins may be utilized to sense the voltage across the bridge via a reference sense amplifier whose output may be applied via Analog Function Card Connector J1, Pin 1, to control the DPI reference. The differential output of the bridge may be scaled, offset, or amplified, or may be applied directly to the differential inputs. As described above, the scaling resistor between Pins 6 and 18 of J3 converts the output to arbitrary engineering units.



Analogic Application Engineers would be pleased to provide additional examples and assistance to OEM users.

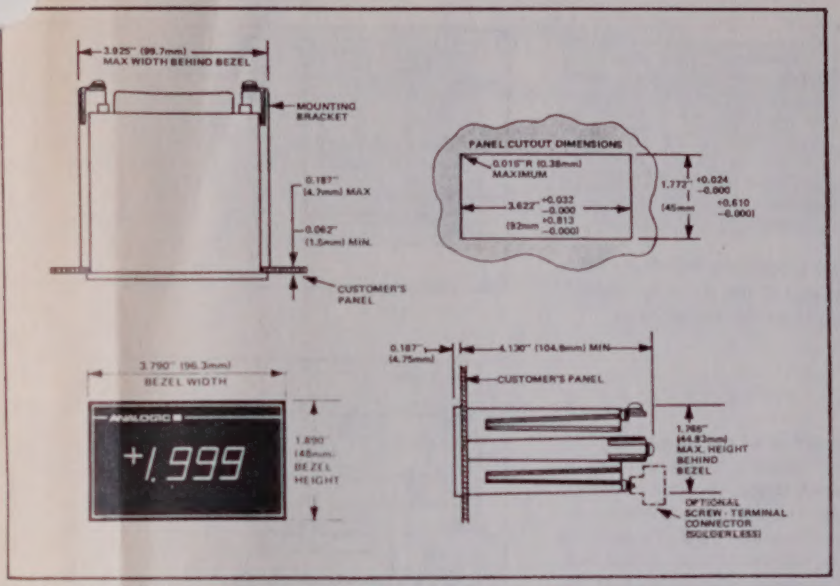


Figure 8. Panel Mounting and Outline Dimensions

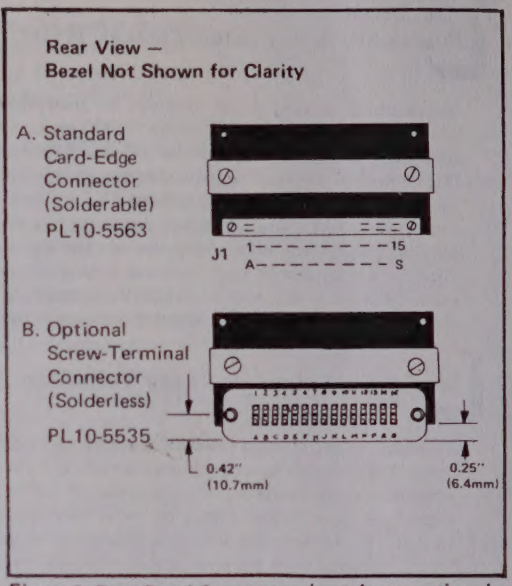


Figure 9. Rear Panel Connectors (metal case option shown)

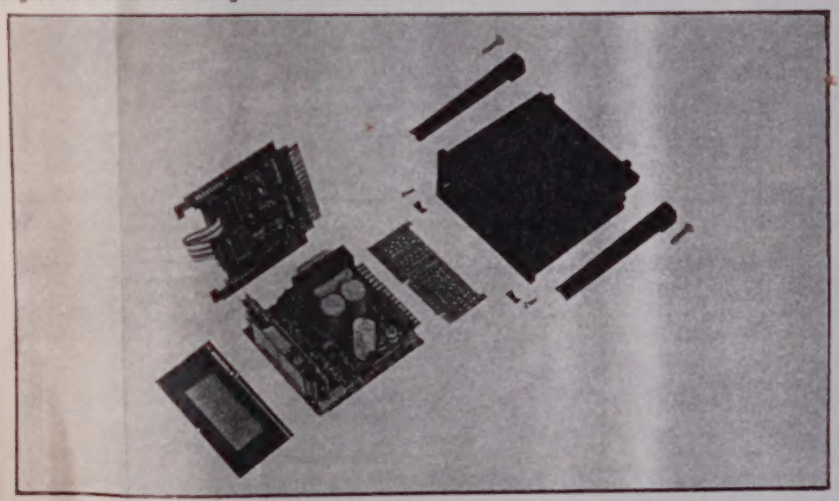


Figure 10. Complete DPI and Additional Function Cards

For LED displays only, either one (1DZL) or two (2DZL) "dummy" zeros may be added to the right end of the digital readout. These zero digits are "fixed"; that is, they always display "0" (1DZL) or "00" (2DZL) for all input signals within the specified range.

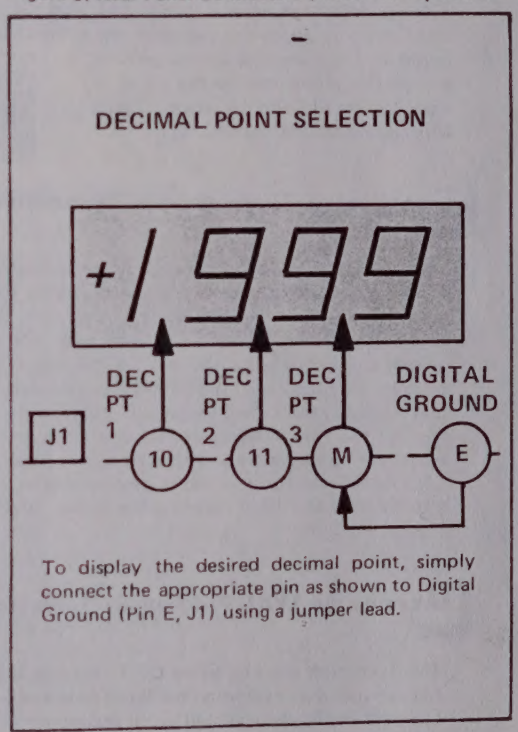
Specify For	–1DZL*	–2DZL*
1999 Range	+1.9990	+1.99900
3999 Range	+3.9990	+3.99900

Dummy Zeros

*Add to end of Order Code. Factory installation only.

**For positive inputs, negative sign does not light. For overload inputs, decimal point and middle horizontal segments of dummy zeros are lit; negative sign lights for negative overload only.

Figure 11. "Dummy" Zero Display



To display the desired decimal point, simply connect the appropriate pin as shown to Digital Ground (Pin E, J1) using a jumper lead.

Figure 12. Decimal Point Position Terminals

NEED APPLICATIONS HELP?

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